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Detailed Insight into the CZTS/CdS Interface Modification by Air Annealing in Monograin Layer Solar Cells

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ABSTRACT: Relatively fast achievements in the kesterite solar cell technology have been made over the last decade, but the experimental efficiency is still ~13%. One proposed reason is an inappropriate band alignment with Cu_2ZnSnS_4 (CZTS) and CdS that results in strong interface recombination losses. Results of this work show that the temperature and duration of air annealing of the CZTS/CdS heterojunction are essential for device performance. Soft annealing slightly improved the device efficiency due to the elemental intermixing at the interface. On the other hand, extended annealing increased absorber band gap energy, resulting in higher V_{OC} values, indicating the improved Cu–Zn ordering in the CZTS structure, which also could be expected to have a beneficial influence on the device performance. However, interface analysis revealed that the CZTS absorber surface layer was Cu-rich, providing the reason for the reduction in CZTS solar cell performance. The effect of annealing on the interface defects was analyzed by the capacitance–frequency–voltage (C–V–f) analysis combined with SCAPS simulations. C–V–f-based loss maps showed that air annealing modifies the density distribution of asymmetrical interface states at the CZTS/CdS interface, which becomes fully symmetrical for longer annealing times at 200 °C.

KEYWORDS: kesterite, Cu_2ZnSnS_4, interface, solar cells, air annealing
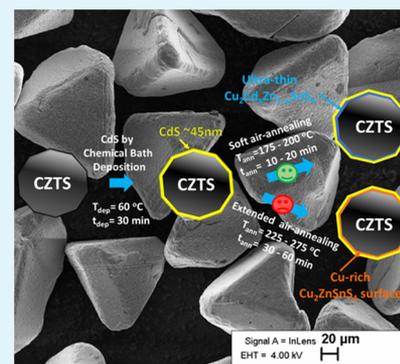
1. INTRODUCTION

Cu_2ZnSnS_4 (CZTS) is highlighted as a potential semiconductor compound for absorber material in photovoltaics having p-type conductivity, high absorption coefficient, and adjustable band gap. The crystal structure of kesterite is very similar to chalcopyrite $Cu(In,Ga)Se_2$ (CIGS). Thus, combining the suitable properties of absorber and the similar device structure,[1] relatively fast development has been made with kesterite solar cells and the highest efficiency of 12.6% for CZTSSe-based thin-film solar cells has been presented by the IBM group in 2013[2] and recently renewed by Zhou et al. in 2021.[3]

The most implemented buffer layer in CZTS thin-film solar cells is still CdS deposited by the chemical bath deposition (CBD) method, which has been proven as a simple, fast, and inexpensive technique to produce uniform and reproducible thin films. There are several advantages of using a buffer layer—absorber surface protection against damage from the high-energy ZnO sputtering process; chemical etching of the surface in the CBD process; and Cd diffusion by modifying surface composition. The last feature is associated with a Cu-poor absorber surface layer that leads to a replacement of Cu^+ by Cd^{2+} due to their closely matched ionic radii: 0.97 and 0.96 Å, respectively.[4,5] In the CIGS material, this process causes a change in conductivity type in the surface layer by moving the

junction into the absorber; thus, the minority carriers from the bulk become majority carriers at the device interface, having there a lower recombination rate.[6,7] There have not been found such inversion of conduction type in the CZTS surface region, and therefore, the p–n junction is located at the CZTS/CdS interface.[8] With a high-band-gap kesterite like Cu_2ZnSnS_4, the band alignment between the absorber and CdS is poor and results in strong interface recombination losses. It directly affects the device performance.[9] CZTS solar cells have shown a negative band offset, so-called "cliff-like", in which the conduction band minimum (CBM) of CZTS is higher than that of CdS.[10] According to theoretical calculations, the negative value of conduction band offset (CBO) limits open-circuit voltage (V_{OC}) and fill factor (FF) due to recombination at the heterojunction interface. Both the position of the p–n junction at the CZTS/CdS interface and the negative CBO lead to a much more pronounced dependence of the electrical characteristics of the device on
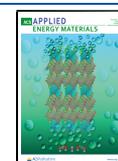
the quality of the CZTS/CdS interface due to interface-related and tunneling-assisted recombination.[8]

The post-annealing of the CZTS/CdS interface shows the potential for the high-performance device. Several groups reported that annealing a CZTS/CdS sample in a different atmosphere—in vacuum,[11] in air,[12,13] or in inert gas[9,14]—is an effective approach to improve the quality of the interface. It was found that postannealing improved the device performance through the passivation of interfacial defects and the reduction of nonradiative recombination. It is also reported that postannealing between 200 and 300 °C could cause an interdiffusion of Cd and Zn, forming a thin layer of $Cu_2Cd_xZn_{1-x}SnS_4$ on the CZTS surface together with an ultrathin $Zn_{1-x}Cd_xS$ layer in between CZTS and CdS.[14−16] These intermediate layers were proposed to change the "cliff-like" band alignment to a "spike-like" band alignment between the absorber and the buffer layer. In addition, donor defect Cd_{Cu} could form as the Cd atoms from CdS occupy the Cu vacancies at the CZTS surface; this will help the inversion in the CZTS surface, thus minimizing the defect-induced recombination loss.[13,16] In a recently published study,[17] Cd doping was found to suppress the formation of Zn-related secondary phase and Cu_{Zn} antisite defects, resulting in the increase of V_{OC} and FF values. Since substitution of Zn by Cd increases the lattice constant of CZTS,[18] it can decrease lattice parameters mismatch between CZTS and CdS, by reducing the interface recombination at the CZTS/CdS interface and promoting future progress in device performance.[17]

This work reports a detailed analysis of the effect of air annealing of CZTS/CdS on the interface properties and on the performance of CZTS monograin layer (MGL) solar cells. The temperature-dependent $J−V$ and admittance spectroscopy measurements were performed to collect more information about the electrical behavior of the devices. The elemental interdiffusion after an air annealing of the CZTS/CdS heterojunction was studied by X-ray photoelectron spectroscopy.

2. EXPERIMENTAL SECTION

Cu_2ZnSnS_4 monograin powder was synthesized from binary compounds—CuS, ZnS, and SnS with purity (99.999%) in the liquid phase of potassium iodide (KI) flux material in a sealed quartz ampoule at 740 °C. The temperature of the muffle furnace was increased from room temperature (RT) to 740 °C within 3 h, and it was kept at an elevated temperature for 142 h. The growth process was terminated by naturally cooling the ampoule to RT in air. As the flux material was water-soluble, the powder crystals were removed from the salt with deionized water. The released powder was dried in a Memmert drying oven at 50 °C, after which the powder was sieved into several narrow granulometric fractions between 38 and 125 μm. More details about the monograin powder growth process are reported in ref 19.

Before using the powder grains as the absorber material in monograin layer solar cells, the powder was etched with 1 vol % Br in methanol for 5 min and then with 10 wt % KCN aqueous solution for 5 min at RT. The objective of chemical etching is to clean the crystal surfaces from the residues precipitated from molten KI.[20] After the etching process, the CZTS powder was heat-treated in a sealed ampoule in a dual-temperature zone furnace at 840 °C in sulfur vapor (p_S = 2000 Torr) for 60 min to heal the surface and adjust the bulk composition of crystals. The CdS buffer layer was deposited on the post-treated powder crystals by the chemical bath deposition method using a vertical rotator in a hot-air thermostat at 60 °C for 30 min. The 360° multifunctional vertical rotator provides compact and uniform CdS coverage on CZTS crystals. An alkali deposition solution

containing 0.01 M cadmium iodide (CdI_2), 1 M thiourea (SC-$(NH_2)_2$), and 2 M ammonia aqueous solution (NH_4OH) was added to adjust the bath solution pH to 11.6 at room temperature. The thickness of the CdS buffer layer was ∼45 nm using the above-mentioned process conditions. Directly after the buffer layer deposition, the CdS-covered CZTS powder was divided into equal parts and air-annealed at temperatures from 175 to 275 °C for 10 to 120 min.

2.1. Solar Cell Fabrication. The schematic structure of the monograin layer solar cell Au/CZTS/CdS/i-ZnO/ZnO:Al is presented in Figure 1. First, monograin membranes were prepared
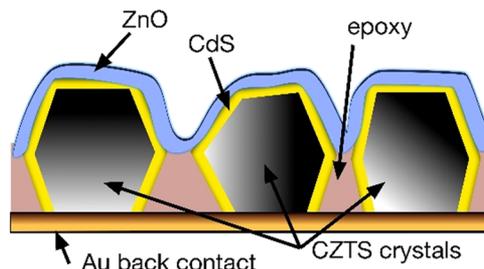

Figure 1. Schematic structure of monograin layer solar cell.

by embedding the CdS-covered CZTS crystal pathway into a low-shrinkage epoxy resin layer on supporting foil. After curing of epoxy, the membranes were covered with a transparent conductive oxide (TCO) layer (i-ZnO and ZnO:Al) by radio-frequency magnetron sputtering. The TCO layer was coated with highly conductive Ag nanowires (Ag-NWs) to improve the conductivity and carrier collection of ZnO. Complete monograin membrane with all of the layers was glued onto a durable transparent substrate. The supporting foil was removed from back side, and for rear contacting, the bottom side of the MGL was abraded with ultrafine sandpaper (Grit size P2500) to remove polymer from powder crystals. With this process, a p^+ layer on the back side of the crystals is created. This type of back contact helps hole tunneling from absorber bulk into metal contact (Au). Metal contacts were thermally evaporated through the metal stencils. The total area of the single cell was 4.5 mm².

2.2. Device Characterization. The current *versus* voltage ($J−V$) characteristics of monograin layer solar cells were measured with a Keithley 2400 source meter under standard test conditions (AM 1.5, 100 mW cm⁻²) using a Newport Oriel Class A 91195A solar simulator. The external quantum efficiency (EQE) was measured using a computer-controlled SPM-2 prism monochromator. The generated photocurrent was detected at a 0 V bias voltage at RT using a 250 W halogen lamp and a DSP lock-in amplifier. The temperature-dependent measurements were performed in the closed-cycle He cryostat. The admittance spectra were recorded using a Wayne Kerr 6500B impedance analyzer, and temperature-dependent $J−V$ curve measurements were made using a Keithley 2401 source meter. Impedance Z and phase angle y were both measured as functions of frequency from 20 Hz to 10 MHz and temperature, which was varied from 20 to 320 K with a step ΔT = 10 K. The amplitude of AC voltage was 30 mV to maintain the linearity of the response signal. Temperature-dependent admittance measurements (AS) were carried out with DC bias of 0 and −0.5 V in the dark. The same setup was used also for room-temperature bias-dependent admittance spectroscopy measurements. CZTS/CdS interface compositional changes were analyzed by a Kratos Analytical AXIS Ultra DLD XPS spectrometer. To collect the signal of photoexcited electrons, the CZTS powder covered with CdS mounted on a rotational sample holder by ultrahigh vacuum-proof carbon tape was excited by monochromatic Al Kα X-ray source (1486.6 eV) at 15 kV and 150 W. The hybrid lens mode in conjunction with aperture slot view (400 × 800 μm) and pass energy 40 eV was set to collect the high-resolution photoelectron spectra. A charge neutralizer was kept on during all XPS measurements. To study the chemical composition of CdS in depth and down to the interface between buffer and absorber
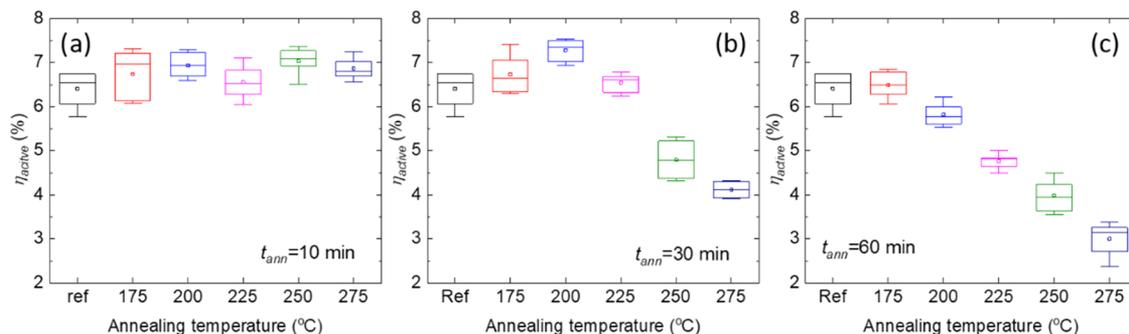
Figure 2. Comparison of solar cell efficiencies after air annealing of CZTS/CdS at different temperatures for (a) 10, (b) 30, and (c) 60 min.
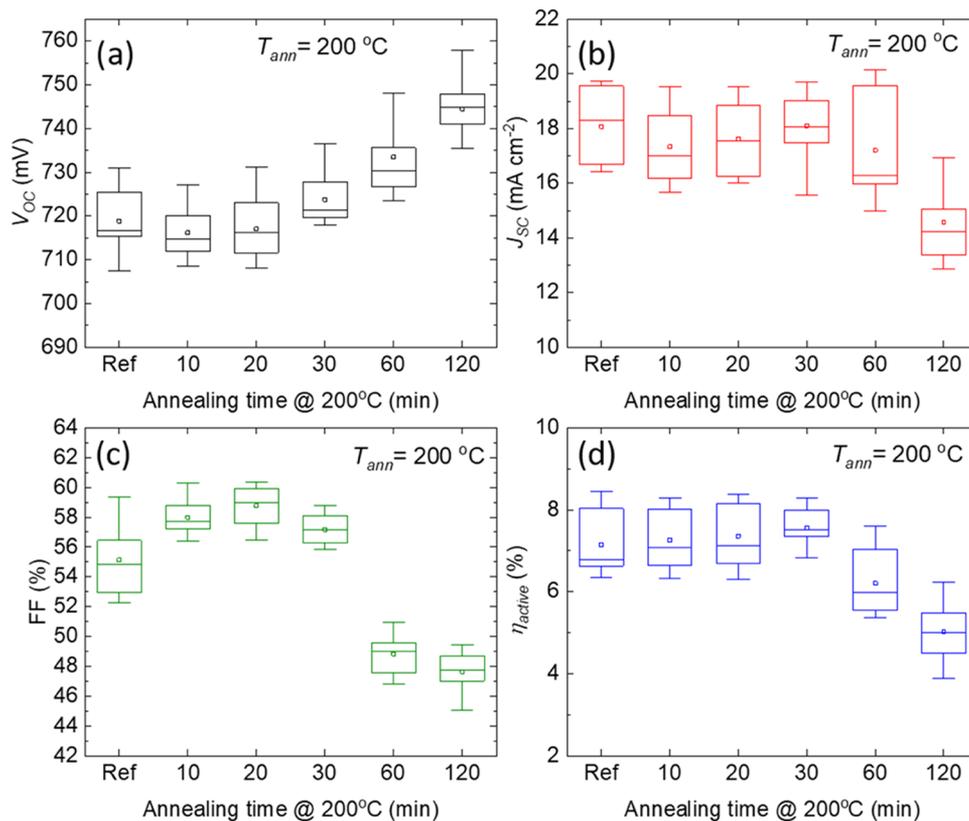

Figure 3. Box plot diagram of (a) open-circuit voltage, (b) current density, (c) fill factor, and (d) efficiency of CZTS devices with CdS annealing in an air at 200 °C for different times.

material, a MiniBeam I Ar$^+$ ion sputtering source was applied at 2 keV and 10 mA. During the removal of the surface layer, the sample holder rotation was turned on at a moderate speed to have a more even surface removal of powder samples.

3. RESULTS AND DISCUSSION

First, air annealing of CdS at different temperatures was performed and its effect on the solar cell parameters was studied. In Figure 2, the influence of 10, 30, and 60 min CZTS/CdS air annealing at different temperatures on the device performance is shown as box plots. Due to the epoxy between the CZTS crystal in the membrane, the active area of the MGL solar cells is around 75% of the total area;[21] therefore, the MGL solar cell efficiency has been converted to active area (η_{active}).

Short-time annealing (t_{ann} = 10 min) in the temperature range of 175–275 °C improved the efficiency from 6.7 to 7.3%. By increasing the annealing time up to 30 min, the

device performance was improved up to 7.5% at temperatures 175–200 °C. Annealing at 225 °C and higher temperatures for 30 min was detrimental for solar cell efficiencies. Annealing for a longer time (t_{ann} = 60 min) showed slightly higher efficiencies for solar cells based on the CZTS/CdS heterojunction that were annealed at 175 °C. Annealing at 200 °C and higher temperatures was already detrimental for solar cell performances. From these results, it was concluded that CZTS/CdS air annealing at 200 °C is beneficial for improving the performance of MGL devices.

As a next step, more precise investigations using different annealing times at 200 °C were performed to understand the annealing effects on the device performance. The photovoltaic parameters of CZTS devices based on the heterojunction annealed in air at 200 °C for different times are presented as box plots in Figure 3. The average value is calculated from 15 solar cells. The average V_{OC} values increased from 717 to 743 mV by extending the annealing time to 120 min (Figure 3a).

The average j_{SC} value 18.1 mA cm^{-2} was constant until the annealing time was increased to 60 min (Figure 3b). The average FF value decreased from 57 to 48% if the annealing time was longer than 30 min (Figure 3c).

However, the main parameters of solar cell are not the only data we can extract from J−V characteristics. For example, the light J−V curve analysis can be used to evaluate the quality of the p−n junction and losses related to resistive components of the device. In this study, the single exponential diode equation was employed to analyze the light J−V data. The diode parameters including the series resistance (R_s) and the diode ideality factor (n) found from these analyses are plotted in Figure 4. Series resistance decreases from 2.8 to 1.8 Ω cm^2 by
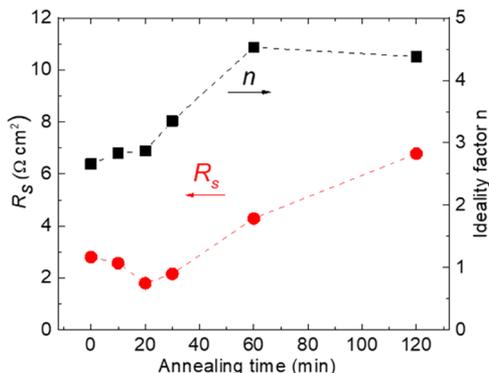

Figure 4. Photovoltaic parameters R_s and n for CZTS MGL solar cells based on air-annealed CdS at 200 °C for different times (one-diode model fitting results).

annealing at 200 °C up to 20 min and then starts to increase again. Ideality factor is around n = 2.6−2.8 for devices without annealing and annealing at 200 °C for 10 and 20 min. Longer-time annealing at 200 °C degrades the quality of solar cells, and the n value increases over 4.4−4.5, which is seen also in degraded FF values indicating high recombination losses.

For more information about the electrical properties of the cells, temperature-dependent J−V measurements were carried out under illumination. The behavior of the V_{OC} of the cells as a function of temperature, V_{OC} (T), is shown in Figure 5a and can be described by the following equation[22]

$$V_{OC} = \frac{E_a}{q} - \frac{Ak_BT}{q}\ln\left(\frac{J_{00}}{J_L}\right) \tag{1}$$

where E_a is the activation energy, q is the elementary charge, A is the idealify factor, k_B is the Boltzmann constant, T is the temperature, J_{00} is the reverse saturation current prefactor, and J_L is the light generated photocurrent density. At relatively high temperatures (above 200 K), V_{OC} versus T shows linear behavior. The extrapolation of this linear part to T = 0 K indicates the activation energy E_a. According to eq 1, the calculated E_a values of these devices are all smaller than the band gaps of their absorbers extracted from the EQE spectra (Figure 5b), which indicates that there is recombination at the heterojunction interface of these solar cells.

As mentioned, EQE measurements were used to estimate the band gap (E_g) values of CZTS absorber materials by plotting the (EQE)^2 vs E. From the linear segment of the low-energy side of the construction curves, the effective band gap energy (E_g^*) can be extracted. The estimated E_g^* values increased from 1.568 to 1.619 eV (ΔE_g = 51 meV) by CZTS/CdS heterojunction annealing at 200 °C longer than 60 min. Estimated band gap energy values from EQE for absorbers and the corresponding CZTS device parameters (E_a, V_{OC}, and $V_{OC\,def}$) based on annealed heterojunctions at 200 °C for different times are summarized in Table 1. The V_{OC} deficits are

Table 1. Effective Band Gap Energy, Activation Energy, Open-Circuit Voltage, and V_{OC} Deficit for CZTS Monograin Layer Solar Cells with Different CdS Annealing Times at 200 °C

t_{ann} at 200 °C [min]	E_g^* [eV]	E_a [meV]	V_{OC} [mV]	$V_{OC\,def}$ ($E_g^* - V_{OC}$) [mV]
w.o.	1.568	1320	731	837
10	1.567	1295	732	835
20	1.564	1263	731	833
30	1.571	1246	736	835
60	1.609	1175	748	861
120	1.619	1185	757	862

calculated in this paper with respect to the effective band gap energy values from EQE. Then, $V_{OC\,def} = E_g^* - V_{OC}$. It is seen that although the V_{OC} values increase with a longer annealing process, the V_{OC} deficit remains large or even becomes larger by considering the band gap increase.

One reason for the band gap increase could be the existence of the ordering−disordering phenomenon in kesterites. First-principles calculations have shown that ordered and disordered kesterite phases have the band gap energy difference around
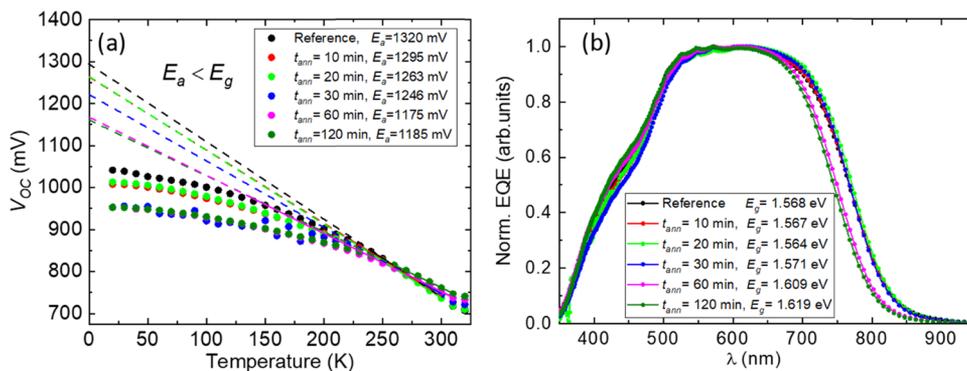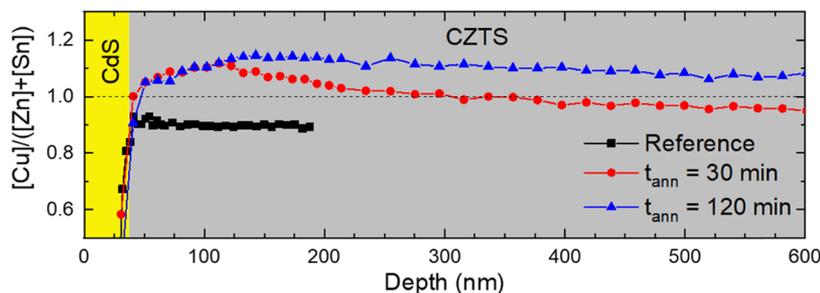

Figure 5. (a) Temperature-dependent V_{OC} of CZTS monograin layer solar cells and the linear fits showing the extrapolation to T = 0 K for the determination of E_a and (b) EQE spectra of the corresponding cells.

Figure 6. XPS elemental depth profiles of heterojunction without and with 30 and 120 min air annealing at 200 °C.

100 meV in CZTS.[23] Photoluminescence (PL) studies have shown that the PL band energy is about 80 meV smaller for disordered structures than from the same radiative recombination of ordered structure.[24] Transition between ordered and disordered CZTS could be done using low-temperature postannealing at temperatures below the critical temperature ($T_c \sim 260$ °C), and the degree of disordering depends on annealing time.[25] Our results show that CZTS/CdS annealing at 200 °C up to half an hour is beneficial to improve the FF values, which can be attributed to reduced series resistance (R_s). A longer-time CZTS/CdS annealing probably reduces the degree of disordering in CZTS, resulting in CZTS absorber material with a higher band gap,[26] but at the same time, we see an increase of recombination losses at the interface. PL study showed that change in the degree of disordering changes also the radiative recombination mechanism from band to tail to deep defect related recombination, which in most ordered material could reduce its positive effect to the CZTS solar cell performance.[26]

We also studied the elemental interdiffusion induced by annealing of the CdS/Cu$_2$ZnSnS$_4$ heterostructure in air at 200 °C for different times. X-ray photoelectron spectroscopy elemental depth profiles of samples before and after air annealing at 200 °C for 30 and 120 min were determined. To reveal the changes in the CZTS absorber material surface composition, the [Cu]/([Zn] + [Sn]) ratios were calculated and are presented in Figure 6 (yellow area is CdS (∼35 nm) and gray area is the surface of CZTS monograins (∼550 nm)).

XPS depth profiles of [Cu]/([Zn] + [Sn]) revealed that air annealing at 200 °C for 30 and 120 min resulted in the formation of a Cu-rich ([Cu]/([Zn] + [Sn]) > 1) CZTS absorber surface close to the interface. The Cu-rich absorber surface layer thickness was found to increase with annealing time. Out-diffusion of Cu from the absorber is a well-known phenomenon in the Cu-chalcogenide/CdS heterojunction.[27] Cu has the highest mobility, and its out-diffusion into the CZTS surface could be the reason for the formation of the Cu-rich surface. To consider the phase diagram Cu$_2$S-ZnS−SnS$_2$,[28] there exists a Cu-rich CZTS phase to some extent (few mol %). So, we propose that air annealing results in Cu-rich CZTS on the surface, but not the formation of secondary phases. It is known that Cu-poor and Zn-rich CZTS absorber composition is needed for high-efficiency devices.[29,30] Therefore, we propose that despite the reduction in the degree of Cu−Zn disordering leading to improved V_{OC} and increased E_g with longer-time annealing as presented in Table 1, it is not beneficial for the device performance due to the formation of a Cu-rich absorber surface.

A slight improvement in the performance of the CZTS MGL solar cells after short-time annealing at 200 °C could also be

due to the possible formation of an ultrathin Cu$_2$Cd$_x$Zn$_{1−x}$SnS$_4$ layer at the CZTS/CdS interface or due to improved CdS crystallinity, but it was not possible to provide solid evidence of the Cd diffusion into CZTS by XPS.

To further look into the recombination mechanisms in the studied solar cells, admittance spectroscopy (AS) was implemented. AS inspects the current response of a solar cell to small AC bias voltage modulation and its dependence on frequency f and temperature T, presumably due to the capture and emission of the electrically active defects. In a simple single-junction device, it is possible to extract defect parameters such as activation energy, capture cross section, and density of states.

The capacitance of the solar cell is a superposition of the free carrier capacitance across the width of the space charge region (SCR) C_d and the influence from the charging and discharging of deeper defect levels within the SCR of the $p−n$ junction. If deeper traps are present, the band bending in the SCR causes the Fermi level E_F to cross the trap level E_t at some distance from the interface, at the crossing point x_t. The AC voltage with the frequency f produces the electric charge stored by traps to oscillate in the vicinity of x_t. The trapped electric charge tracks the AC voltage oscillations and contributes to the total solar cell capacitance only if their frequency does not surpass the specific trap frequency f_t. Therefore, in the case of $f_{lf} \ll f_t$, the trap-related capacitance C_t is equal to C_{lf} where C_{lf} is the low-frequency capacitance, which depends on the trap density N_t and the acceptor concentration N_a if the depletion layer is in the p-type absorber material. In the high-frequency ($f_{hf} \gg f_t$) region, the solar cell capacitance C is determined by C_{hf}, where C_{hf} is the high-frequency capacitance. Accordingly, in the case of a single majority carrier trap level, the overall junction capacitance can be described by the equation[31,32]

$$C(f) = C_d + \frac{C_{lf} - C_d}{1 + (2\pi f)^2 \tau^2} \qquad (2)$$

where τ is the characteristic trapping time of the trap. It is a function of the trap density N_t, the acceptor concentration N_a, and the SCR width w. In the case of a small trap concentration N_t, the specific frequency f_t for the hole trapping defects is $f_t = (2\pi\tau)^{-1}$.[31,32] The inflection frequencies f_t can be determined from maxima in the derivative $-f\, dC/df$ spectra that should exhibit a peak at the frequency f_t. In general, these peaks in the $-f\, dC/df$ graphs could be linked to defect responses, series resistances in the solar cell, or carrier freeze-out.

In the present paper, first, we followed the method developed in ref 33 and measured room-temperature bias- and frequency-dependent capacitances of our CZTS solar cells annealed at 200 °C for different times. The results of solar cell capacitance measurements are represented as 2D contour plots
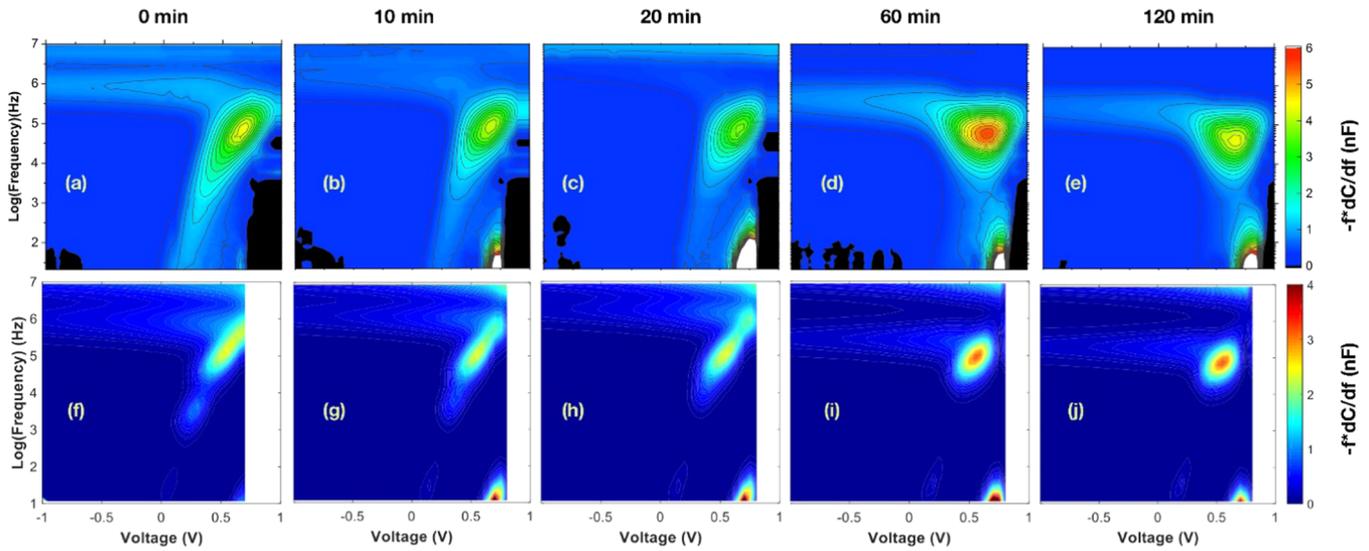
Figure 7. $-f\,dC/df$ Contour plot of the CZTS devices as a function of bias voltage and frequency. Experimental data (a)−(e) and SCAPS simulation results (f)−(j).

showing the derivative of the capacitance with respect to the frequency multiplied by the frequency. These plots can be called "loss maps" because highlighted responses in these contour plots correspond to replies of different nonidealities in the devices; see Figure 7. We see that with increasing annealing time at 200 °C, the rather busy loss maps show a certain modification. The most prominent peak can be found at about 70 kHz and 0.6−0.7 V. We made a temperature-dependent admittance spectroscopy measurement for the 60 min annealed sample to find a depth of this defect state. It is known that the temperature dependence of the inflection frequency f_t is described by the equation:[31]

$$2\pi f_t(T) = e_t(T)/\pi = \pi^{-1} N_{c,v} \nu_{Th} \sigma_{n,p} \exp(-E_A/kT)$$

$$= \xi_0 T^2 \exp(-E_A/kT) \tag{3}$$

where $N_{c,v}$ is the effective density of states in the conduction or valence band, e_t is the emission rate, $\sigma_{n,p}$ is the capture cross section for electrons or holes, ν_{Th} is the thermal velocity of the minority carriers at the interface, $E_A = E_t - E_v$ is the activation energy of the defect level E_t with respect to the valence band edge E_v in p-type absorber, and ξ_0 includes all of the temperature-independent parameters. The activation energy of a defect level E_A can be obtained from the temperature dependence of the capacitance spectra, i.e., from the Arrhenius plot of $\ln(2\pi f_t T^{-2})$ versus $1000/T$. It turned out that the activation energy of this defect is about 155 meV; see Figure 8. Thus, this defect is present in all measured solar cells.

As a next step, the loss map simulations were performed using the SCAPS software.[34] The simulations in SCAPS were performed without external illumination. The capacitance and conductance of the solar cell structure were calculated at the same points as for our experimental data, with 50 different frequency points varying logarithmically from 100 Hz to 1 MHz and with a bias voltage ranging from −1.5 to +1 V with a voltage step of 50 mV. The simulated structure consists of a Au/CZTS/CdS/i-ZnO/ZnO:Al stack. The parameters used in SCAPS simulation for the different layers are summarized in Table 2.

The respective layer thicknesses are 1 μm, 40 nm, 60 nm, and 750 nm, corresponding to the actual physical thickness
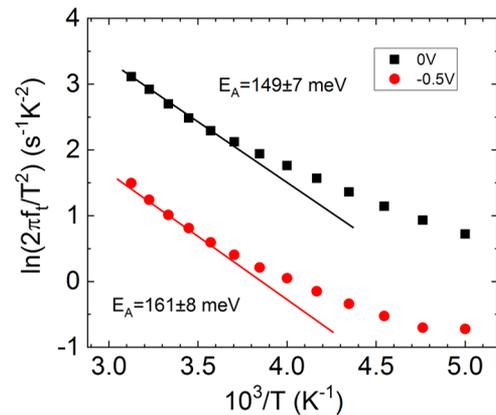

Figure 8. Arrhenius plot of the sample annealed for 60 min showing the calculated activation energies of the defect levels corresponding to capacitance step. Measured at 0 and −0.5 V bias.

Table 2. Properties of the Different Layers in the Simulated Structure

layer	thickness [nm]	carrier density [cm⁻³]	electron affinity [eV]	band gap [eV]
CZTS	1000	2×10^{16}	4.1	1.5
CdS	40	5×10^{17}	4.2	2.4
i-ZnO	60	5×10^{17}	4.4	3.3
ZnO:Al	750	1×10^{20}	4.4	3.3

values of the different layers, with the exception of the CZTS, which is in reality thicker. But 1 μm is a sufficient thickness for the simulation to account for most of the band bending in the device. Different nonidealities were added to the device structure, which are a series resistance of 0.5 Ω cm^2, a back side contact barrier with an activation energy that increases gradually with annealing time, and three different interface state defects at the CZTS/CdS interface. The properties of the three interface state peaks also vary as a function of annealing time. The properties of the different nonidealities and their variation with annealing time are summarized in Table 3.

The different nonidealities in the devices all contribute to a different part of the signal in the loss maps of Figure 6. The

Table 3. Variation of the Different Nonidealities as a Function of Annealing Time

nonidealities		annealing time [min]				
		0	10	20	60	120
back contact barrier	activation energy [eV]	0.33	0.32	0.31	0.36	0.37
interface defect 1	activation energy [eV]	0.155	0.155	0.155	0.155	0.155
	defect density [$cm^{-2}\ eV^{-1}$]	2×10^{12}	2×10^{12}	2×10^{12}	2×10^{12}	2×10^{12}
interface defect 2	activation energy [eV]	0.195	0.185	0.175	0.155	0.155
	defect density [$cm^{-2}\ eV^{-1}$]	8×10^{11}	6×10^{11}	6×10^{11}	6×10^{11}	6×10^{11}
interface defect 3	activation energy [eV]	0.4	0.4	0.4	0.4	0.4
	defect density [$cm^{-2}\ eV^{-1}$]	4×10^{8}	8×10^{8}	8×10^{8}	8×10^{8}	8×10^{8}

series resistance is adding the signal at a frequency of about 10 MHz. The back side barrier is adding the horizontal signal at a frequency of about 1 MHz. The third interface defect with an activation energy of 0.4 eV is adding the signal at 10 Hz and a voltage of about 0.7 V, whereas the other two interface peaks are contributing to the largest signal that is extending over most of the frequency range in forward bias. In fact, in the experimental measurement, this signal seems to be coming from a somewhat asymmetrical interface defect peak, with a maximum at an activation energy of about 0.155 eV and a tail toward deeper activation energies. Unfortunately, in SCAPS, only Gaussian interface defect peaks can be simulated. Therefore, the exact simulation of this response is not possible. We have tried to approximate the experimental data using two Gaussian peaks, a large one at an activation energy of about 0.155 eV and a smaller one at a slightly larger activation energy, simulating the asymmetry of the experimental data toward higher activation energies. The resulting simulated signal in the loss map is not really agreeing completely with the experimental data but is reproducing the correct trend. As the annealing time increases, the asymmetry of the defect peak is reducing, and after 60 min of annealing, the asymmetry has disappeared and the defect peak is fully Gaussian. Therefore, we may conclude from the admittance data analysis that there are several recombination routes in our CZTS MGL solar cells, among which is interface recombination. Unfortunately, none of these routes is disappearing with air annealing of the CZTS/CdS interface at 200 °C for different times ranging from 10 to 120 min. However, the CZTS/CdS heterojunction is modified as the distribution of interface states density at the CZTS/CdS interface becomes symmetrical after 60 min of annealing at 200 °C.

4. CONCLUSIONS

The effect of CZTS/CdS air annealing on the interface properties and on the performance of CZTS monograin layer solar cells was studied. Current–voltage characteristics showed that short-time CZTS/CdS air annealing (t_{ann} = 10 min) at temperatures between 175 and 275 °C slightly improved the efficiency from 6.7 to 7.3% due to the possible formation of an ultrathin $Cu_2Cd_xZn_{1-x}SnS_4$ layer at the CZTS/CdS interface or due to improved CdS crystallinity. The optimal condition for improving the efficiency of CZTS monograin layer solar cells was annealing at 175–200 °C for 20 min. Applying longer annealing times, V_{OC} values increased from 717 to 743 mV and the band gap value increased from 1.57 to 1.62 eV, but all other output parameters degraded. According to the XPS study, air annealing at 200 °C for 120 min resulted in most Cu-rich ([Cu]/([Zn] + [Sn]) > 1) CZTS absorber surface close to the interface, which is proposed as the reason for the degradation of devices. Improved V_{OC} values and increased

E_g* values are due to the reduction of Cu–Zn disordering in CZTS.

Admittance spectroscopy studies showed that the CZTS monograin layer solar cell properties change within the air annealing process. C–V–f measurements and SCAPS simulations indicated the change in the defects distribution at the CZTS/CdS interface. The most prominent interface defect has an activation energy of about 155 meV, and it was present in all samples.

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Author Contributions

M.K.-K. designed the overall experiments and mainly wrote the manuscript. K.T., M.P., and K.M. contributed to the fabrication of absorber materials and CZTS monograin layer solar cells. R.J., J.K., and M.G. contributed to the IV-temp, AS measurements, and analysis. M.D. contributed to XPS and EQE measurements and analysis. G.B. and B.V. performed

SCAPS simulations. All of the authors discussed the results and commented on the manuscript.

Notes

The authors declare no competing financial interest.

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