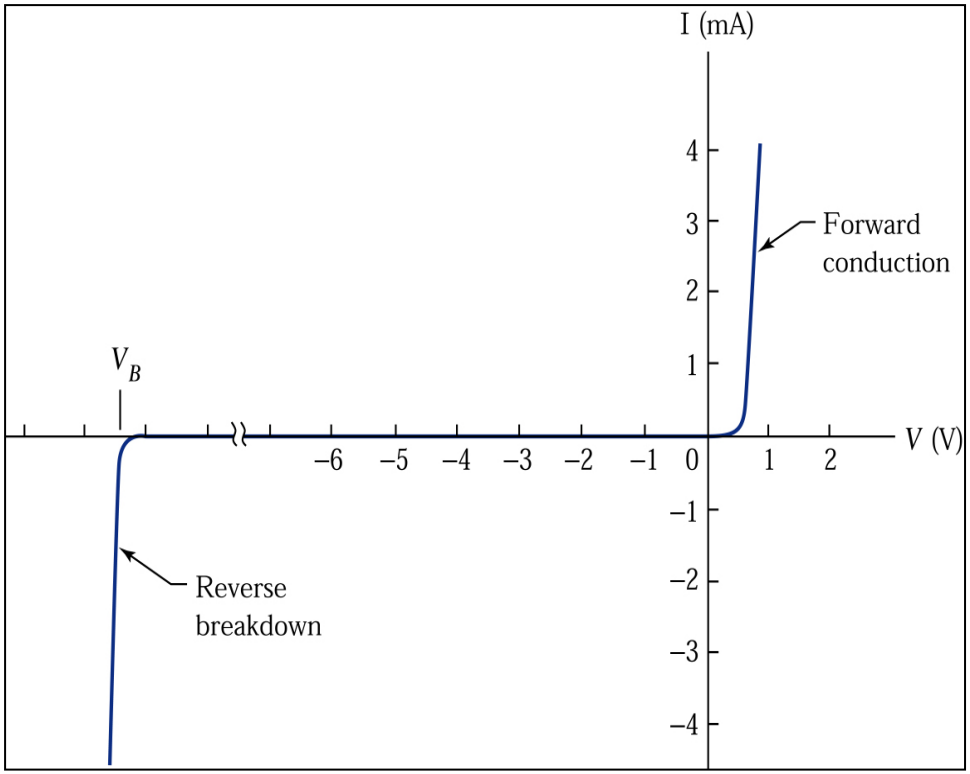
# p-n junction

Diodes, transistors, solar cells.....

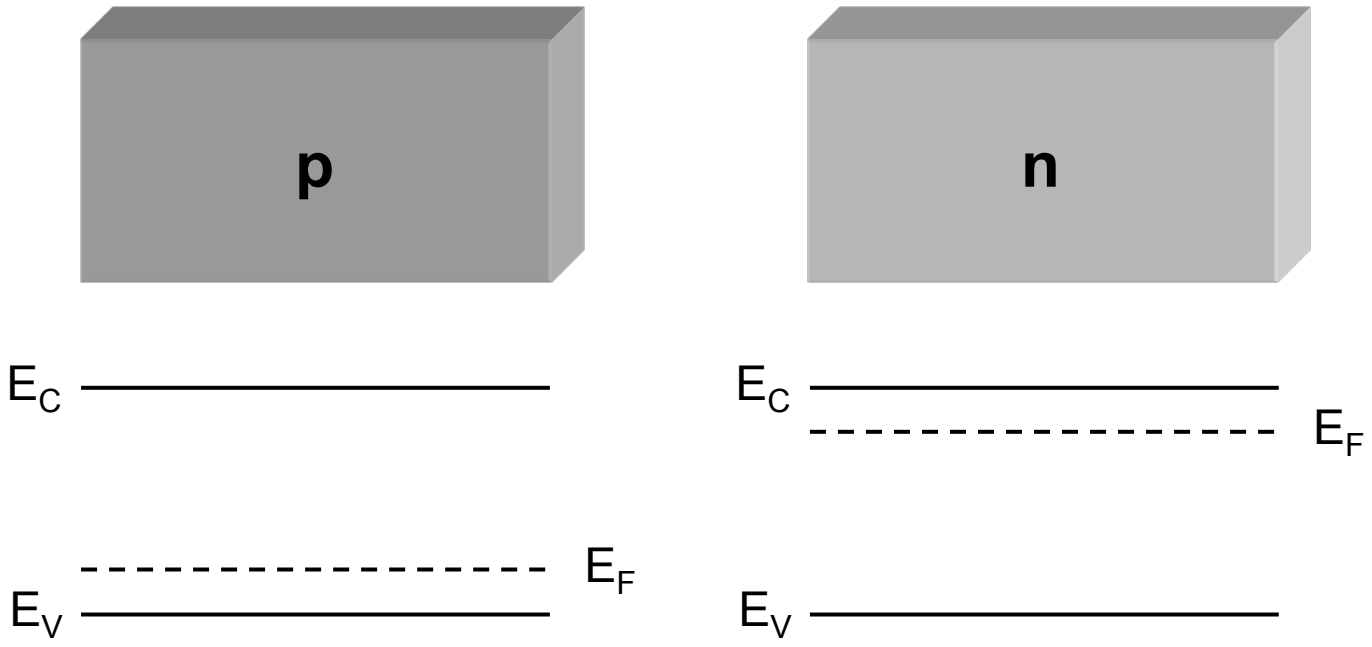
Current flows in one direction!

Reverse bias
(+ sign for n-type)




Forward bias
(+ sign for p-type)

# Formation of p-n junction

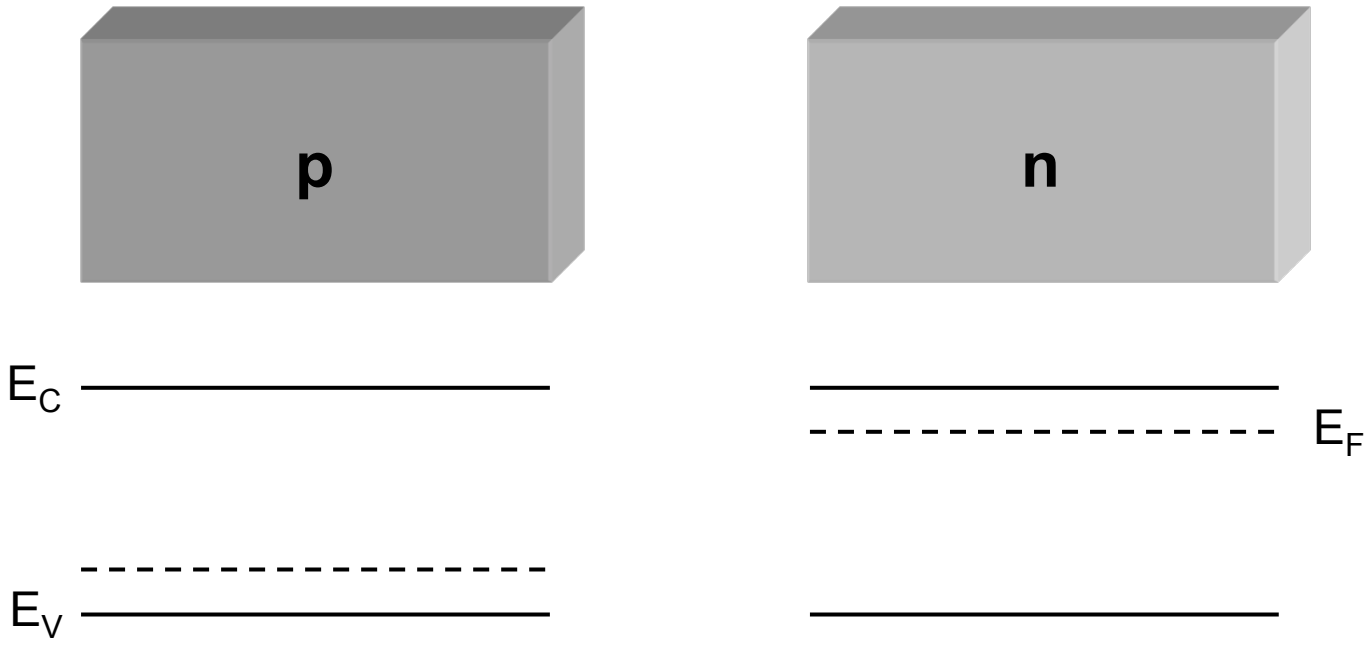



We have p and n-type semiconductors

Position of the Fermi level is different

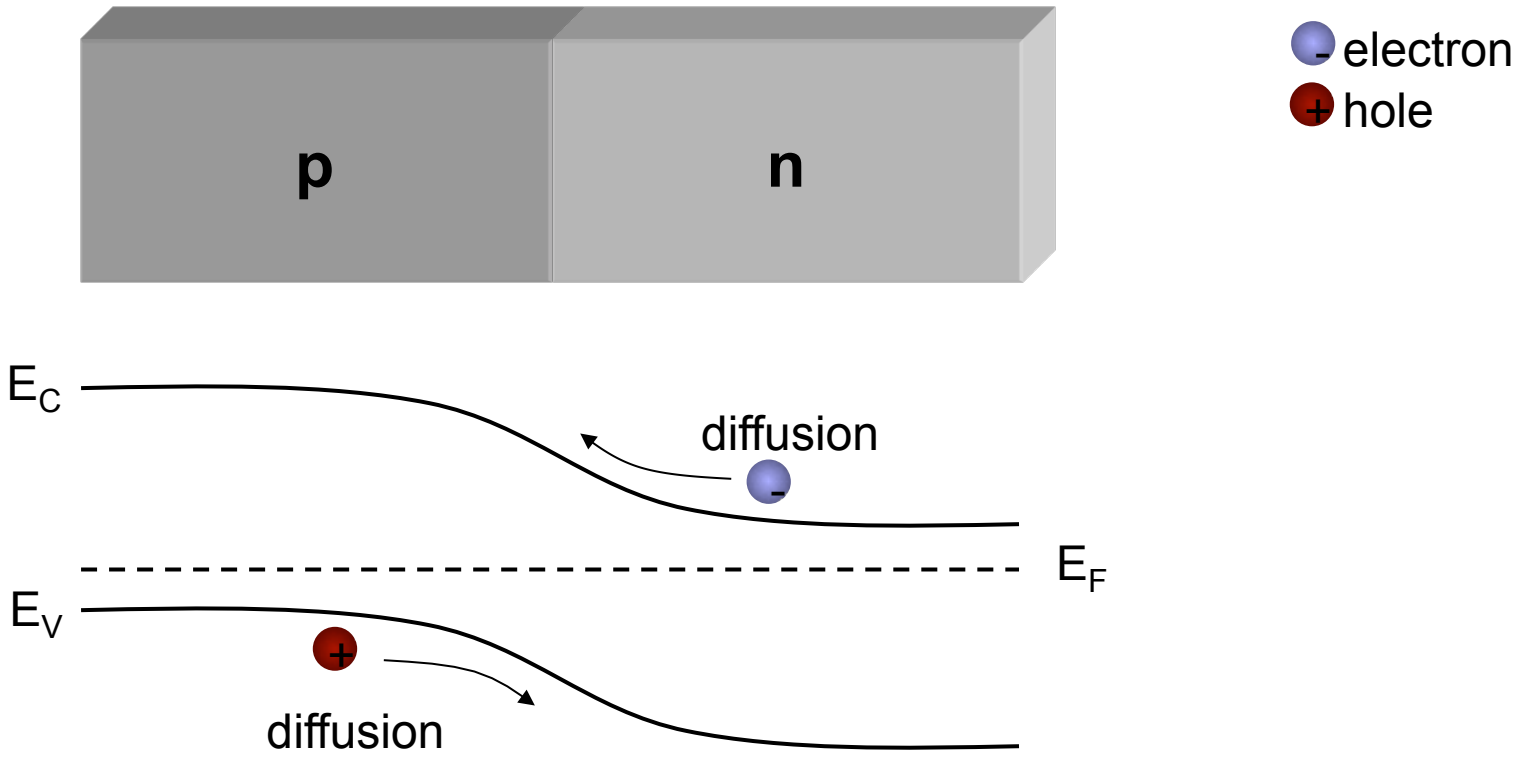
What will happen when we contact both semiconductors?

# Formation of p-n junction



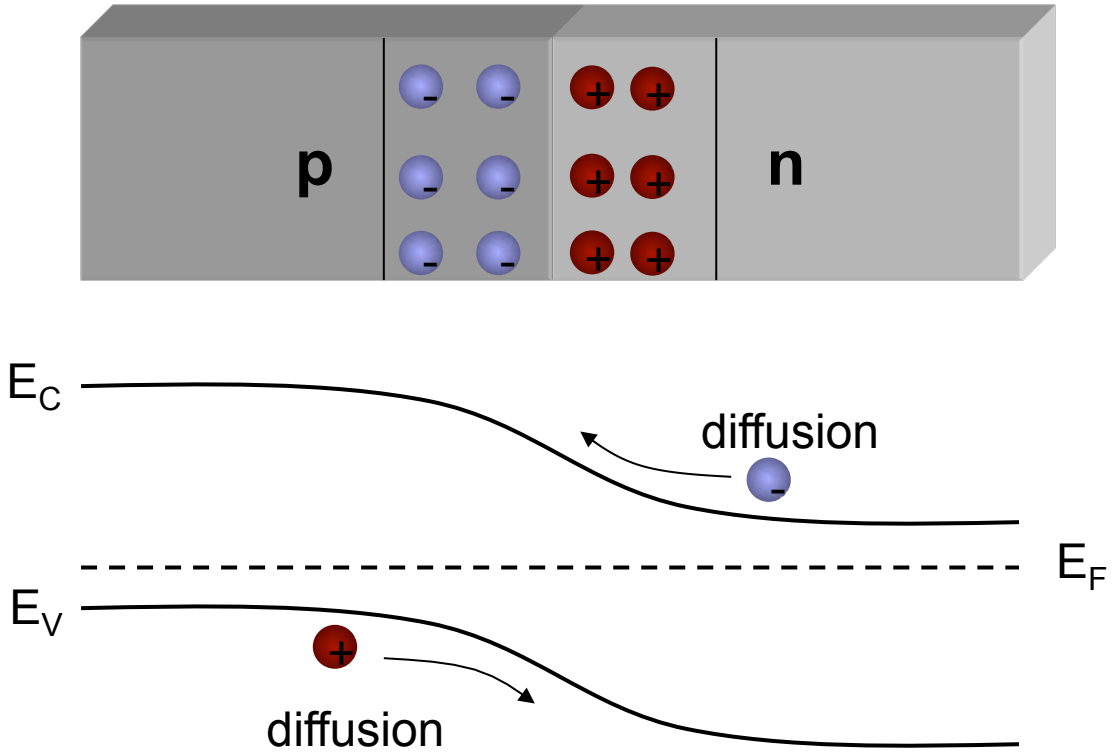

When we do not have any current the Fermi level must be the same on both sides.

# Formation of p-n junction



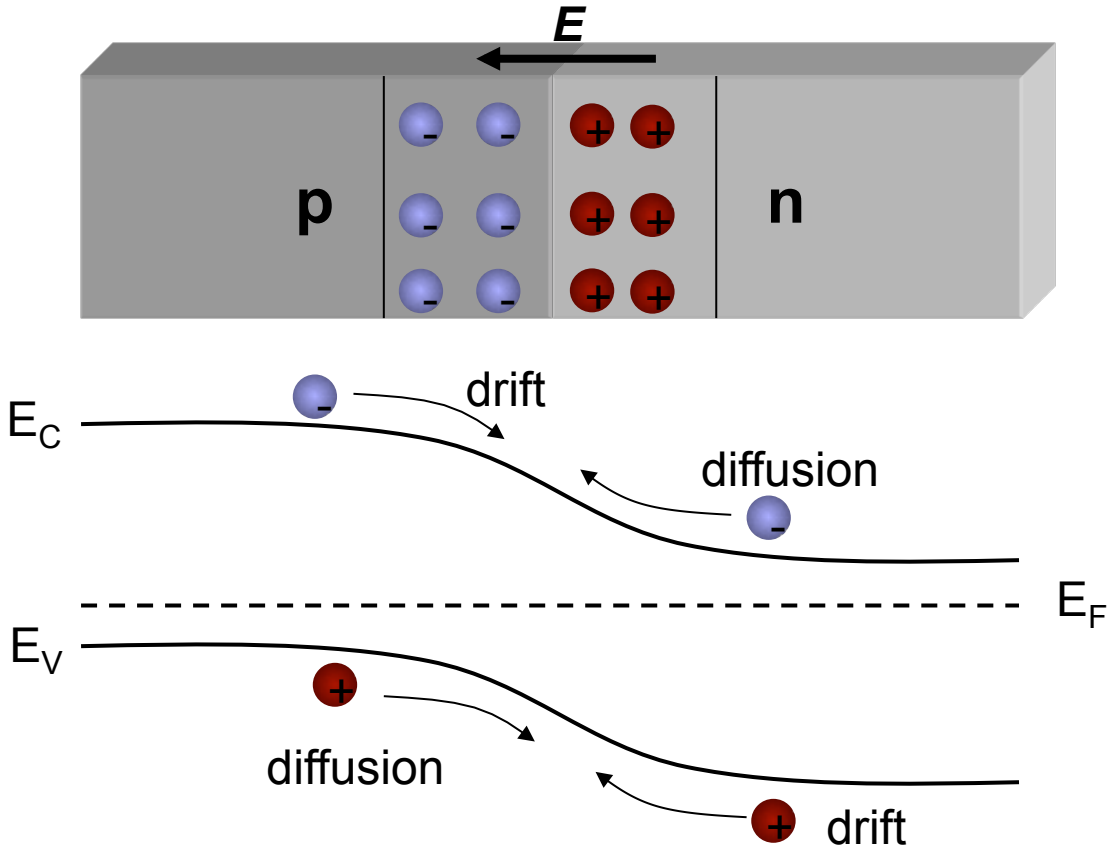

Due to concentration differences there will be a diffusion of holes from p-type to n-type region and vice versa

# Formation of p-n junction




As a result we will have lot of holes in n-type region and lot of electrons in p-type region

# Formation of p-n junction




As a result we will have an electric field *E*.

Due to electric field we start to see also a drift opposite to diffusion

# Some basic assumptions

To describe the properties of a p-n junction we need to know the width of the depletion region, the charge distribution of electrons and holes, and the electric field.

In order to develop a model we need to make some simplifying assumptions,

- The physical junction is abrupt and each side is uniformly doped
- The mobile carrier density within the depletion region is zero
- The transition between the neutral bulk and the depletion region is also abrupt

Armed with these assumptions lets look at the carrier *current* components flowing in the device, the contact potential (or *built in voltage*) and the *width of the depletion region*.

# Carrier current density

When no bias is applied the individual carrier currents due to drift and diffusion cancel each other out.

The hole current density is then given by,

diffusion

$$J_p = e\mu_p pE - eD_p \frac{dp}{dx} = 0$$

drift

$$D_p = \left(\frac{kT}{e}\right)\mu_p$$

Einstein's relation

$$E = \frac{1}{e}\frac{dE_i}{dx}$$

Electric field

by replacing we'll get:

$$\therefore J_p = e\mu_p p\left(\frac{1}{e}\frac{dE_i}{dx}\right) - kT\mu_p \frac{dp}{dx} = 0$$

# Carrier current density

The hole concentration is given by,

$$p = n_i e^{(E_i - E_F)/kT}$$

And therefore it's derivative is,

$$\frac{dp}{dx} = \frac{p}{kT}\left(\frac{dE_i}{dx} - \frac{dE_F}{dx}\right)$$

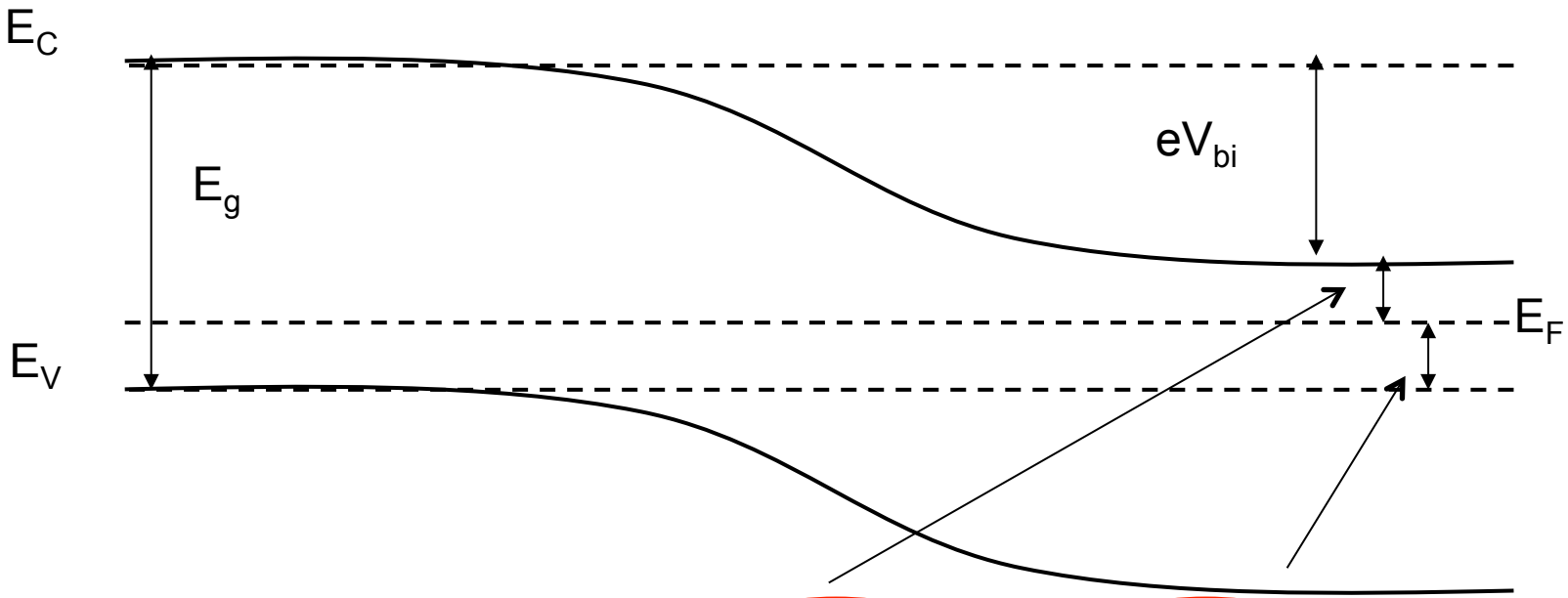
Substitute this into our hole current equation and we see that,

$$J_p = \mu_p p \frac{dE_F}{dx} = 0$$

In other words, proof that at thermal equilibrium with no bias applied, the Fermi level must be constant across the device.

# Built in voltage

As a result of the difference in Fermi level positions when the *p* and *n* type semiconductors are joined, a built-in voltage is produced…




$$eV_{bi} = E_g - \left(E_C - E_F\right)_n - \left(E_F - E_V\right)_p$$

# Built in voltage

We know that the position of Fermi level can be calculated:

$$\left(E_C - E_F\right)_n = -kT \ln\left(\frac{n_n}{N_C}\right)$$

$$\left(E_F - E_V\right)_p = -kT \ln\left(\frac{p_p}{N_V}\right)$$

So we'll get:

$$eV_{bi} = E_g + kT \ln\left(\frac{n_n p_p}{N_C N_V}\right) = E_g - kT \ln\left(\frac{N_C N_V}{n_n p_p}\right)$$

# Built in voltage

We also derived an expression for the intrinsic carrier concentration,

$$n_i^2 = N_C N_V \exp\left(-\frac{E_g}{kT}\right)$$

then Eg will be

$$E_g = kT \ln\left(\frac{N_C N_V}{n_i^2}\right)$$

and the built-in voltage:

$$V_{bi} = \frac{kT}{e} \ln\left(\frac{n_n p_p}{n_i^2}\right)$$

law of mass action

# Built in voltage

If $n_n$ and $n_p$ are the electron densities in the *n*-type and *p*-type regions of the junction, the law of mass action tells us that,

$$n_n p_n = n_p p_p = n_i^2$$

So the built in voltage becomes,

$$V_{bi} = \frac{kT}{e} \ln\left(\frac{p_p}{p_n}\right)$$

$$V_{bi} = \frac{kT}{e} \ln\left(\frac{n_n}{n_p}\right)$$

# Built-in voltage

Conclusions:

- $V_{bi}$ depends on the doping density

$$\boxed{V_{bi} = \frac{kT}{e}\ln\left(\frac{p_p}{p_n}\right)}$$

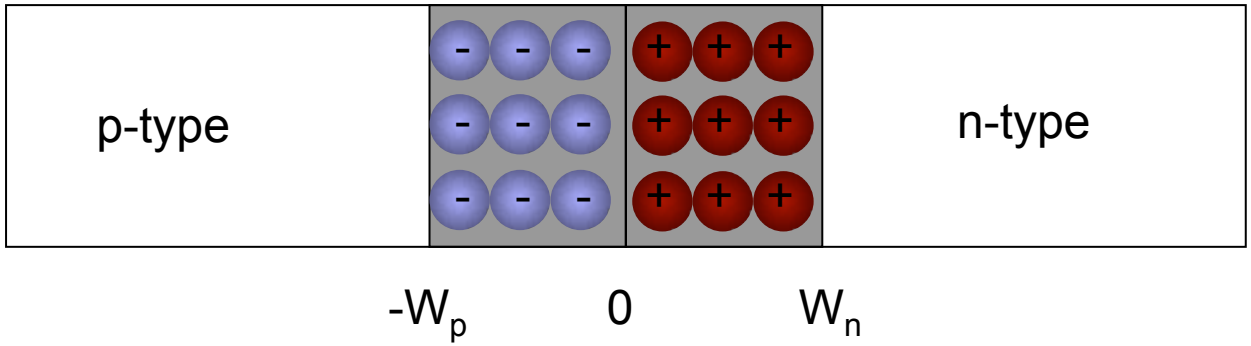
- Maximum $V_{bi}$ is $E_g/e$

$$eV_{bi} = E_g + kT\ln\left(\frac{n_n p_p}{N_C N_V}\right) = E_g - kT\ln\left(\frac{N_C N_V}{n_n p_p}\right)$$

# The depletion region

Let's look closer at the depletion region,

We consider an abrupt junction with no applied bias,




We need to calculate the width of the depletion region,

$$W = W_p + W_n$$

# Poisson's equation

To calculate the width of the depletion region we have to solve Poisson's equation which relates the electrostatic potential $\psi$ and space charge $\rho$ distribution by,

$$\frac{d^2\psi}{dx^2} = -\frac{dE}{dx} = -\frac{\rho_s}{\varepsilon_s} = -\frac{e}{\varepsilon_s}\left(N_D - N_A + p - n\right)$$

Here we assume complete ionisation of donor and acceptor atoms.

# Poisson's equation

Within the p-side depletion region (completely depleted negative space charge region) this simplifies to,

$$\frac{d^2\psi}{dx^2} = \frac{eN_A}{\varepsilon_s} \quad for \quad -W_p \le x \le 0$$

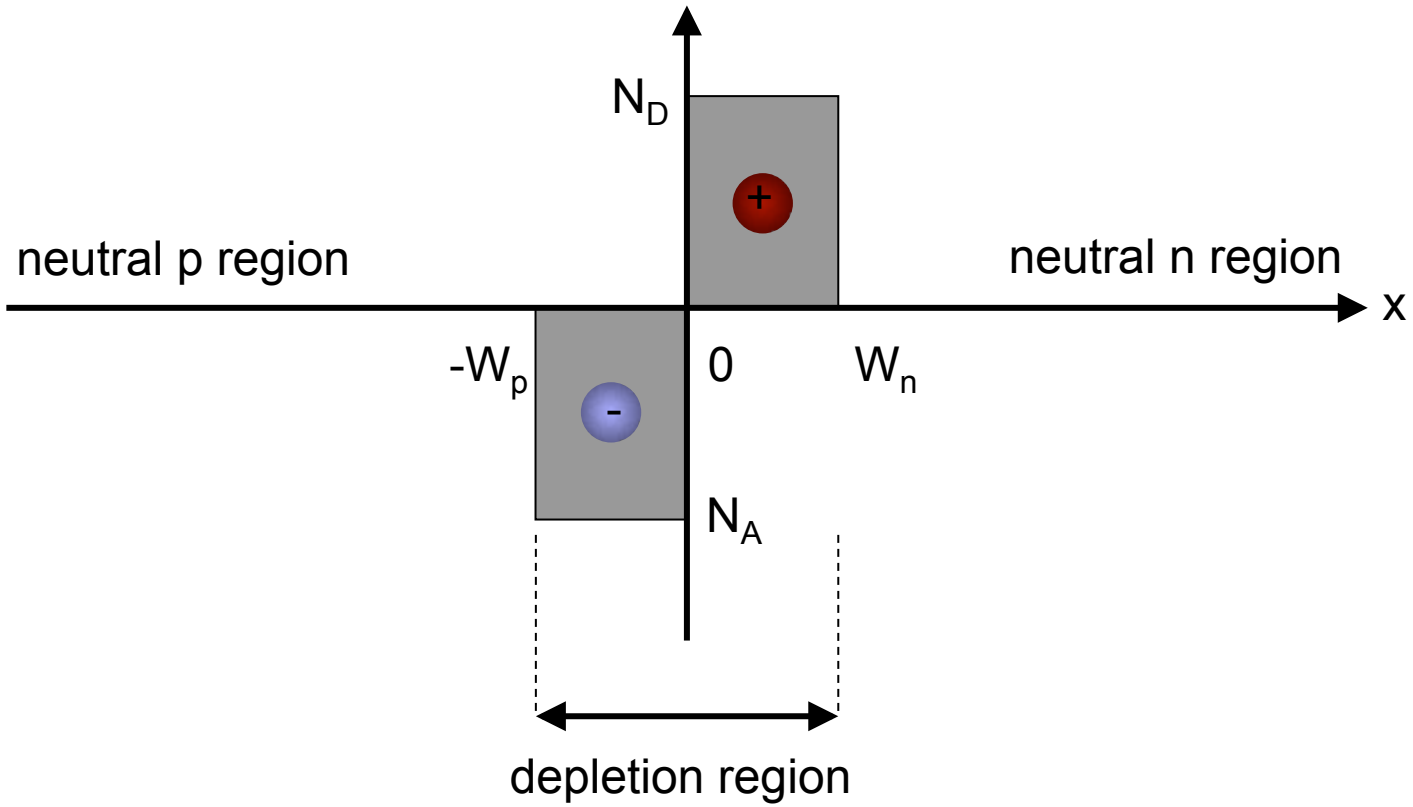
And, within the n-side depletion region to,

$$\frac{d^2\psi}{dx^2} = -\frac{eN_D}{\varepsilon_s} \quad for \quad 0 \le x \le W_n$$

# Space charge distribution

Overall space charge neutrality requires,

$$N_A W_p = N_D W_n$$



# Electric field distribution

If we integrate Poisson's equation we obtain the electric field distribution in the p-side depletion region,

$$E(x) = -\frac{d\psi}{dx} = -\frac{eN_A(x + W_p)}{\varepsilon_s} \quad for \quad -W_p \le x \le 0$$

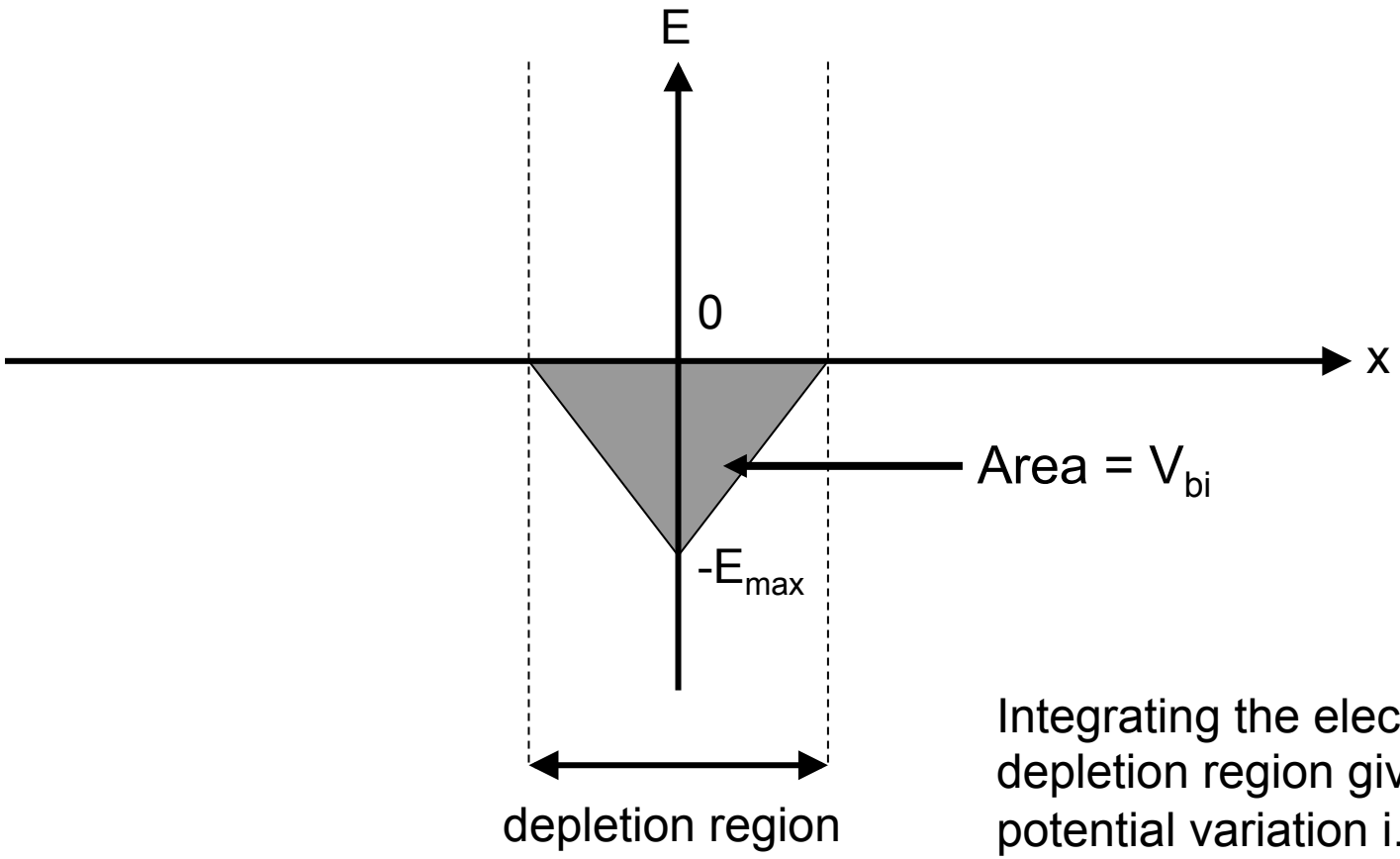
And, within the n-side depletion region,

$$E(x) = \frac{eN_D(x - W_n)}{\varepsilon_s} \quad for \quad 0 \le x \le W_n$$

Electric field is a linear function of x

# Electric field distribution

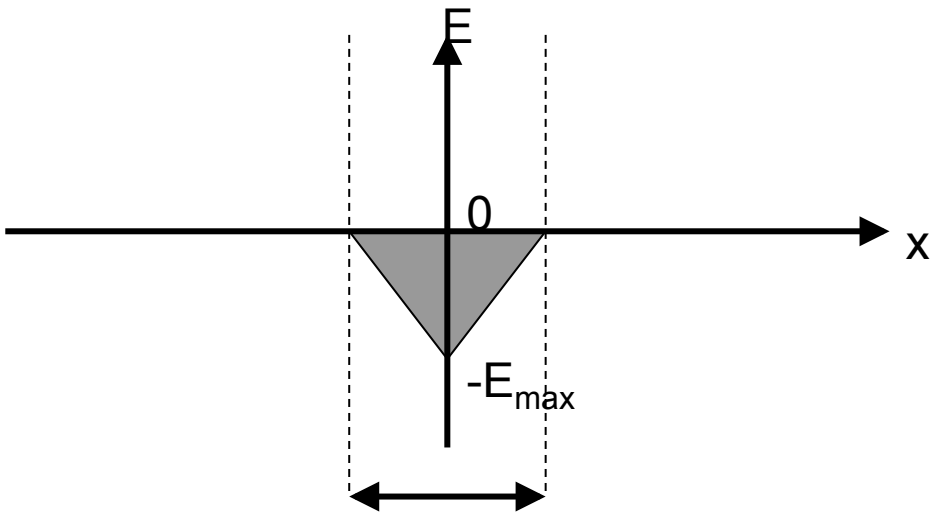
The electric field distribution can therefore be plotted,




Integrating the electric field over the depletion region gives the total potential variation i.e. the built in voltage

# Electric field distribution

At $x=0$ the two regions meet and the field is at its strongest, $E_{max}$




$$E_{\max} = -\frac{eN_A W_p}{\varepsilon_s} = \frac{eN_D W_n}{\varepsilon_s}$$

If we integrate to get the built in voltage,

$$V_{bi} = \int_{-W_p}^{W_n} E(x)\,dx = \frac{eN_A W_p^2}{2\varepsilon_s} + \frac{eN_D W_n^2}{2\varepsilon_s} = \frac{1}{2} E_{\max} W$$

Depletion layer width

# Depletion layer width

Combining these equations we obtain the width of the depletion region as a function of the impurity concentrations and the built in voltage,

$$W_p = \sqrt{\frac{2\varepsilon_s}{e}\left(\frac{N_D}{N_A\left(N_A + N_D\right)}\right)V_{bi}}$$

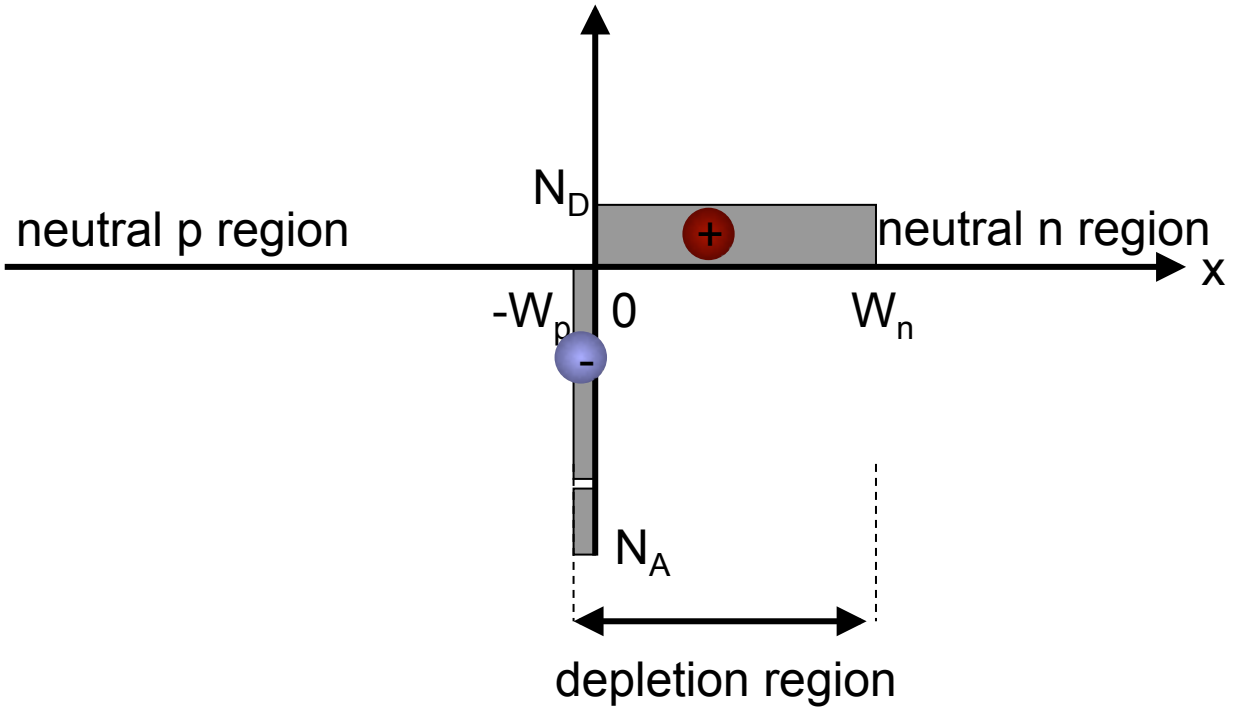
$$W_n = \sqrt{\frac{2\varepsilon_s}{e}\left(\frac{N_A}{N_D\left(N_A + N_D\right)}\right)V_{bi}}$$

$$W = \sqrt{\frac{2\varepsilon_s}{e}\left(\frac{N_A + N_D}{N_A N_D}\right)V_{bi}}$$

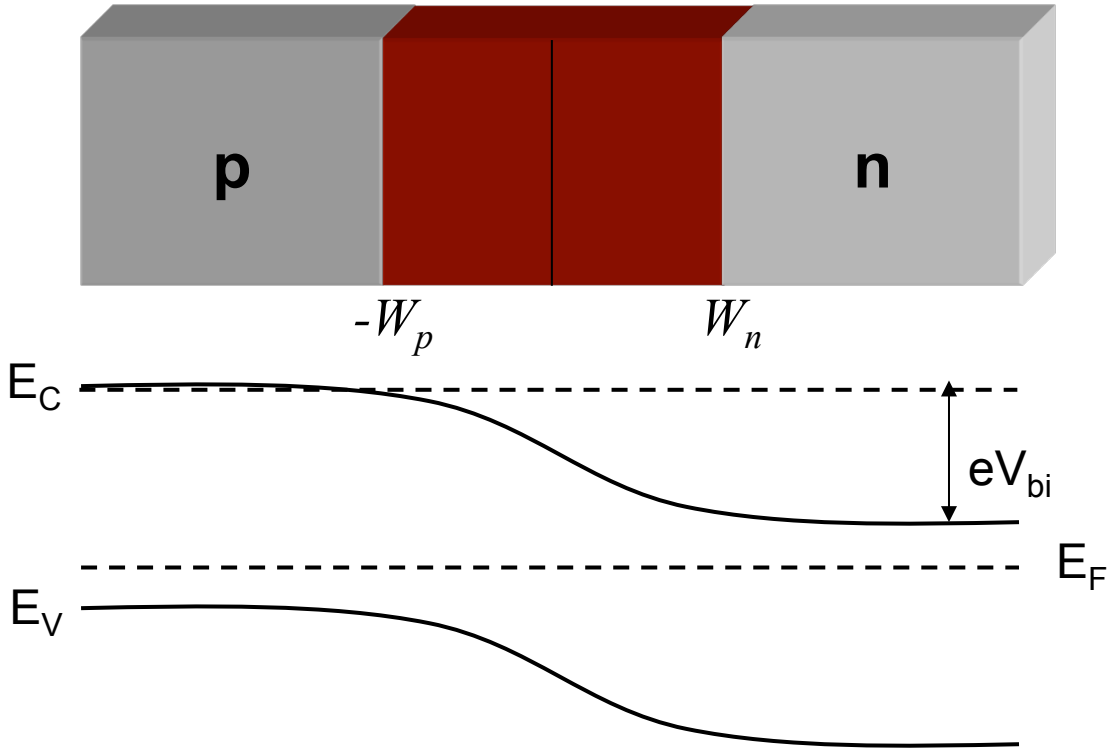
# One-sided abrupt junction

In the case of a one-sided abrupt junction e.g. a $p^+$-$n$ junction where $N_A >> N_D$, the width of the p-side becomes very narrow so that the width of the depletion region is primarily on the lightly-doped n side,

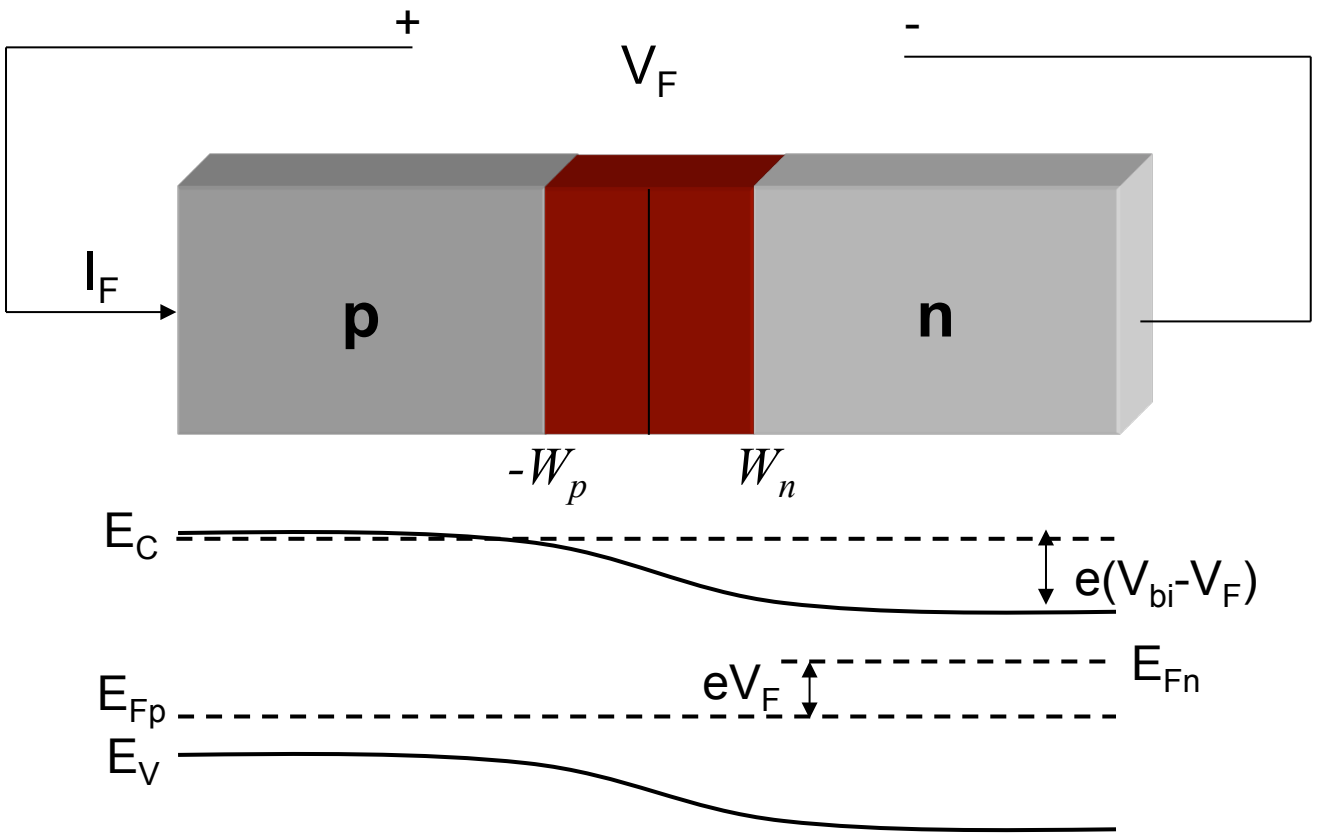
$$W \cong W_n = \sqrt{\frac{2\varepsilon_s V_{bi}}{eN_D}}$$



# Thermal equilibrium



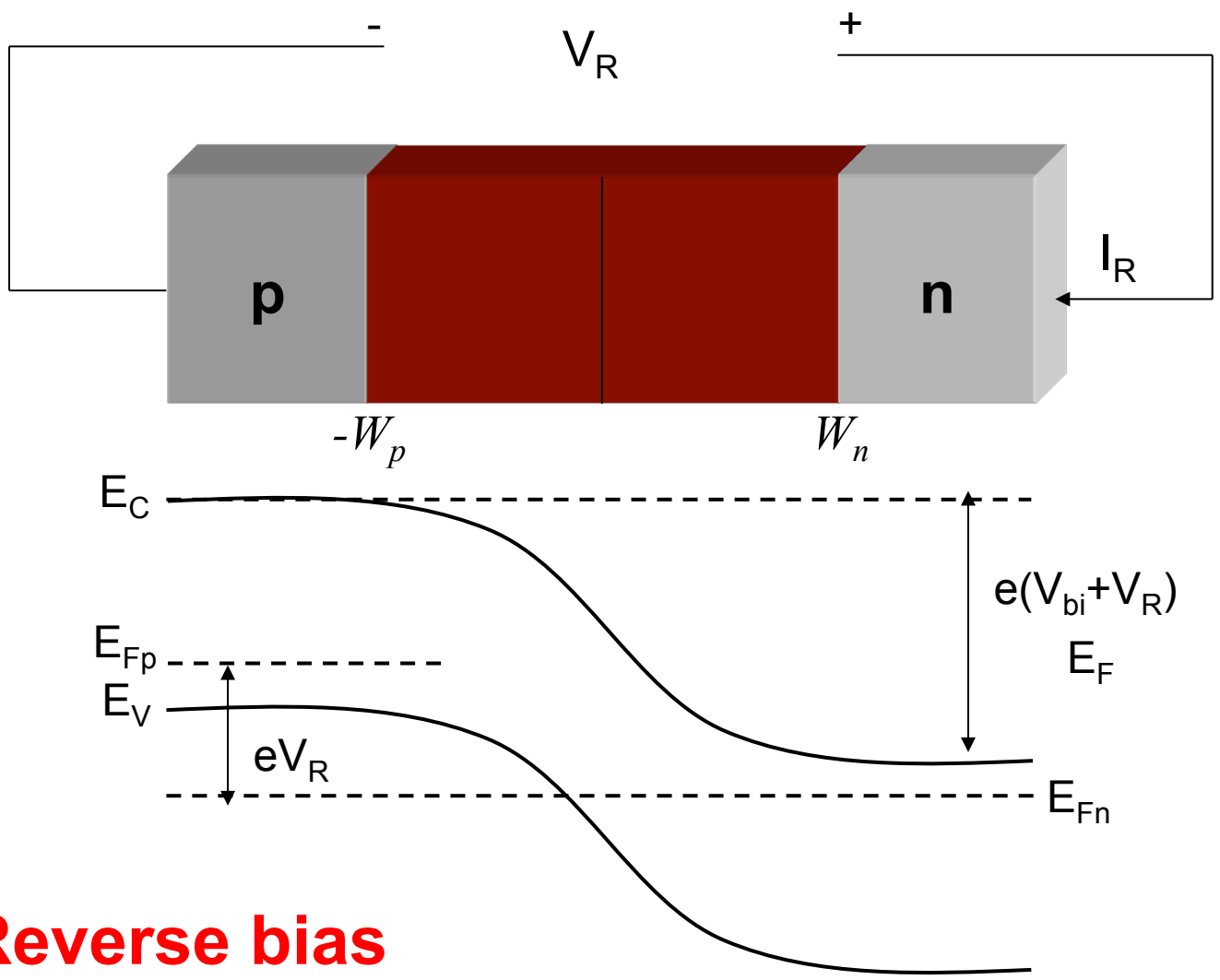

What happens when we apply and external bias across the junction?




# Forward bias

The total electrostatic potential across the junction decreases by $V_F$

Width of the depletion region decreases




## Reverse bias

The total electrostatic potential across the junction increases by $V_R$

Width of the depletion region increases

# Depletion width under bias

V is positive for forward biasing, and negative for reverse biasing so,

$$W = \sqrt{\frac{2\varepsilon_s}{e}\left[\frac{N_A + N_D}{N_A N_D}\right](V_{bi} - V)}$$

So $$W \propto \sqrt{V_{bi} - V}$$

The width of the depletion region varies as the square root of the total electrostatic potential across the junction.

To a good approximation, all of the equations we developed for the *p*-*n* junction at equilibrium can be applied to the junction under bias by replacing $V_{bi}$ with $V_{bi}$-$V$, where $V$ is the applied bias voltage.

# Current flow under bias

## Drift

The presence of an external bias will increase the electric field in the depletion region.

However, under moderate bias conditions, the electric field in the depletion region is always greater than the field required for carrier velocity saturation ($E > 10\ kVcm^{-1}$)…

…a change in the electric field does not alter the drift component of the electron and hole currents…

…all mobile carriers entering the depletion region are swept away and contribute to the same current independent of the field.

# Current flow under bias

## Diffusion

The presence of an external bias will greatly alter the potential energy profile and therefore the gradient of the carrier density across the junction…

…so an applied bias will have a strong effect on the diffusion component of the electron and hole currents

If the hole densities at equilibrium have the relation,

$$\frac{p_p}{p_n} = e^{eV_{bi}/kT}$$

Then under bias *V,*

$$\frac{p(-W_p)}{p(W_n)} = e^{e(V_{bi}-V)/kT}$$

# Current flow under bias

## Diffusion

If we assume low-level injection of mobile carriers, that is the majority carrier densities are essentially unchanged under bias,

$$p(-W_p) = p_p$$

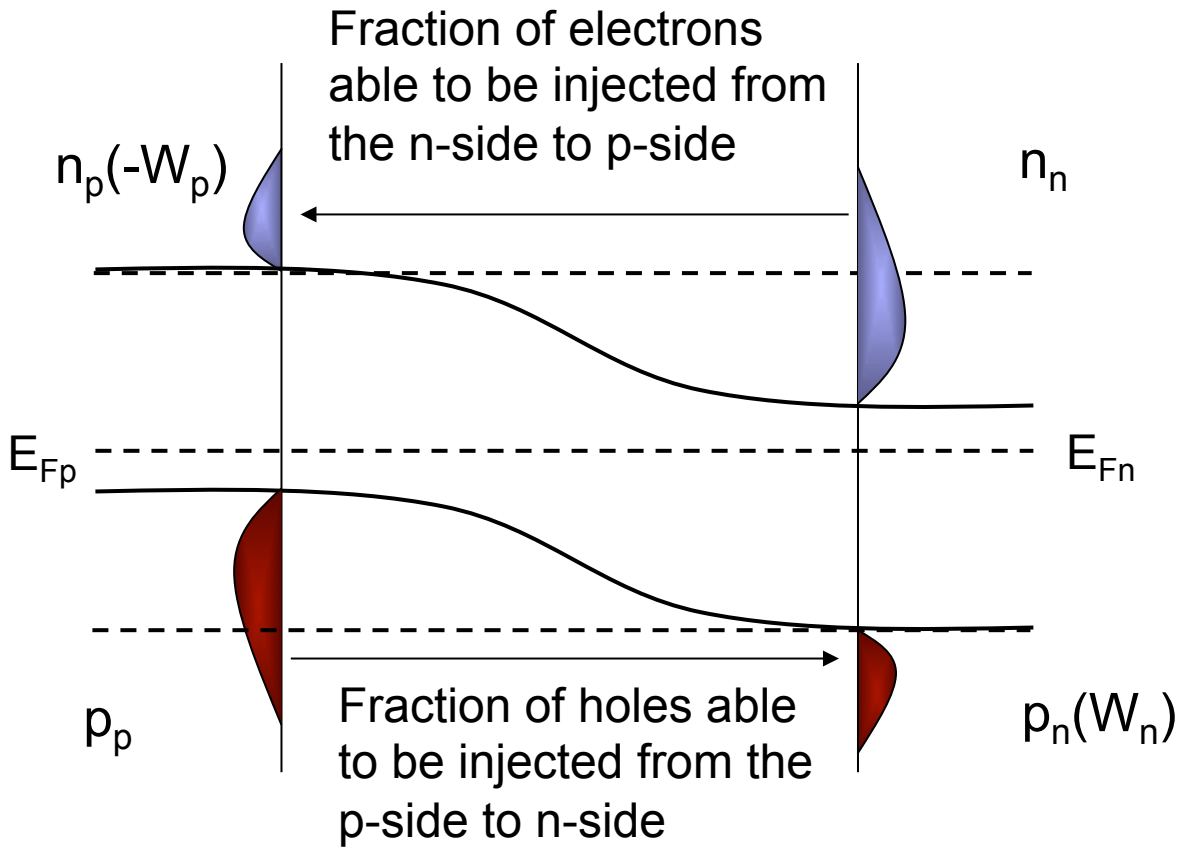
So taking the ratio of the previous two equations we get,

$$\frac{p(W_n)}{p_n} = e^{eV/kT}$$

Only those holes with enough energy to overcome the potential energy barrier $V_{bi}$-$V$ can be injected over from the p-side into the n-side…

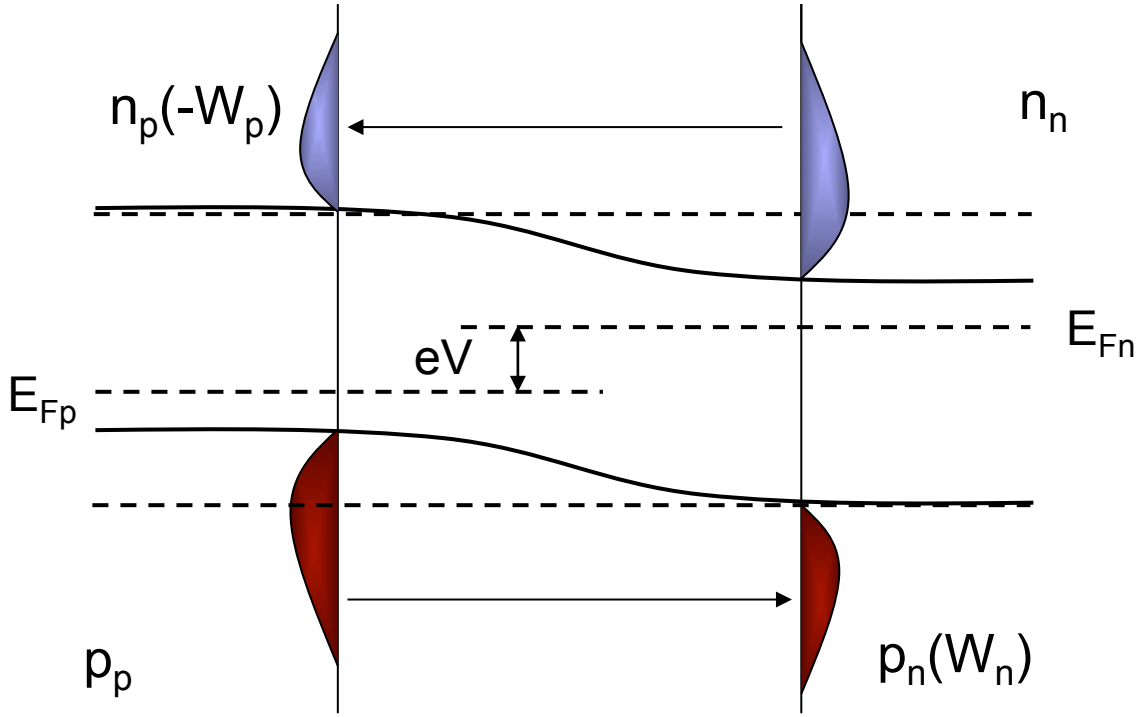
…increase V (forward bias) – decrease the barrier – more holes injected

# Equilibrium (zero bias)



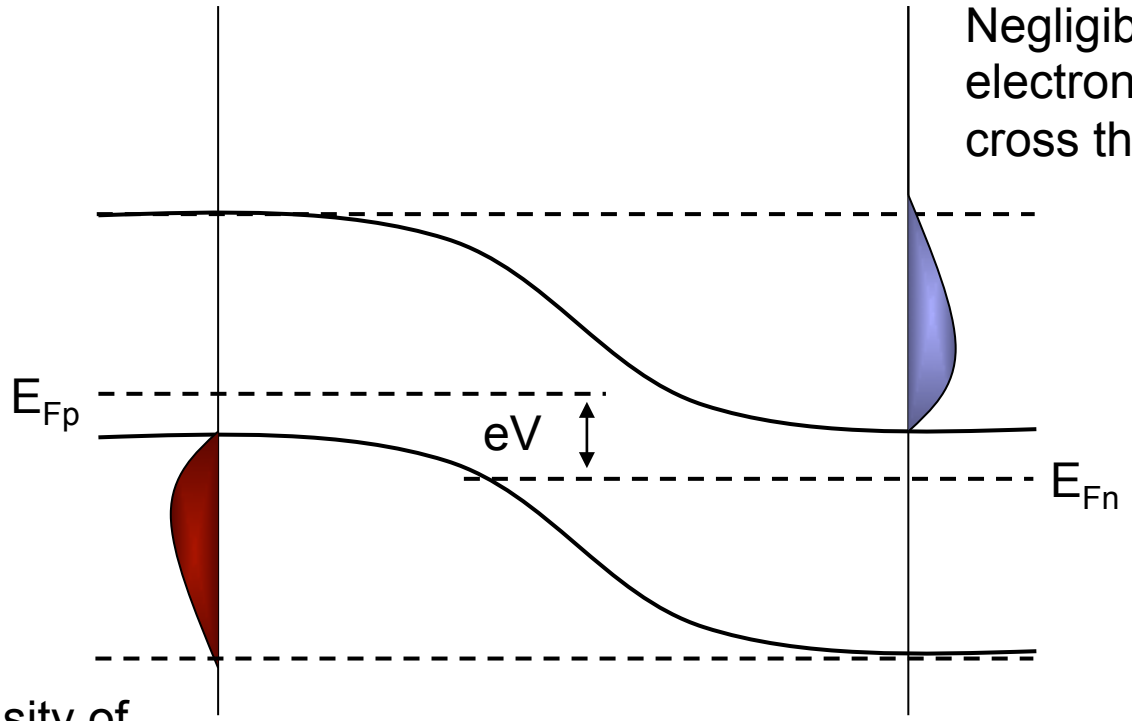

Diffusion current = Drift current

# Forward bias




Diffusion current >> Drift current

# Reverse bias




Diffusion current ~ 0

# Current flow

The excess holes injected across the depletion region is given by,

$$\delta p_n = p(W_n) - p_n = p_n\left(e^{eV/kT} - 1\right)$$

We know from previous that the injected excess minority carrier concentration will decay exponentially into the majority region due to recombination, governed by the diffusion length. The hole density outside the depletion region is then,

$$\Delta p(x) = \delta p_n e^{\left(-(x-W_n)/L_p\right)} = p_n\left(e^{eV/kT} - 1\right)e^{\left(-(x-W_n)/L_p\right)}$$

Similarly for electrons,

$$\Delta n(x) = \delta n_p e^{(x+W_n)/L_p} = n_p\left(e^{eV/kT} - 1\right)e^{(x+W_n)/L_n}$$

# Current flow

Since we assume that the drift current is unaffected by the applied bias, we are now in a position to consider the net current by considering only the diffusion of injected electrons and holes,

$$J_p(x) = -eD_p \frac{d(\Delta p(x))}{dx} = e\frac{D_p}{L_p}(\Delta p(x))$$

The hole current injected into the n-side is proportional to the excess hole density at a particular point. The total current injected into the n-side is given by the current at $x = W_n$,

$$J_p(W_n) = e\frac{D_p}{L_p} p_n \left(e^{eV/kT} - 1\right)$$

# The diode equation

If we assume no recombination in the depletion region, the total current is simply the sum of the hole current injected across $W_n$ and the electron current injected across $-W_p$.

$$J = J_p(W_n) + J_n(-W_p)$$

$$J = J_s\left(e^{eV/kT} - 1\right)$$

Saturation current density

$$J_s = \frac{eD_p p_n}{L_p} + \frac{eD_n n_p}{L_n}$$

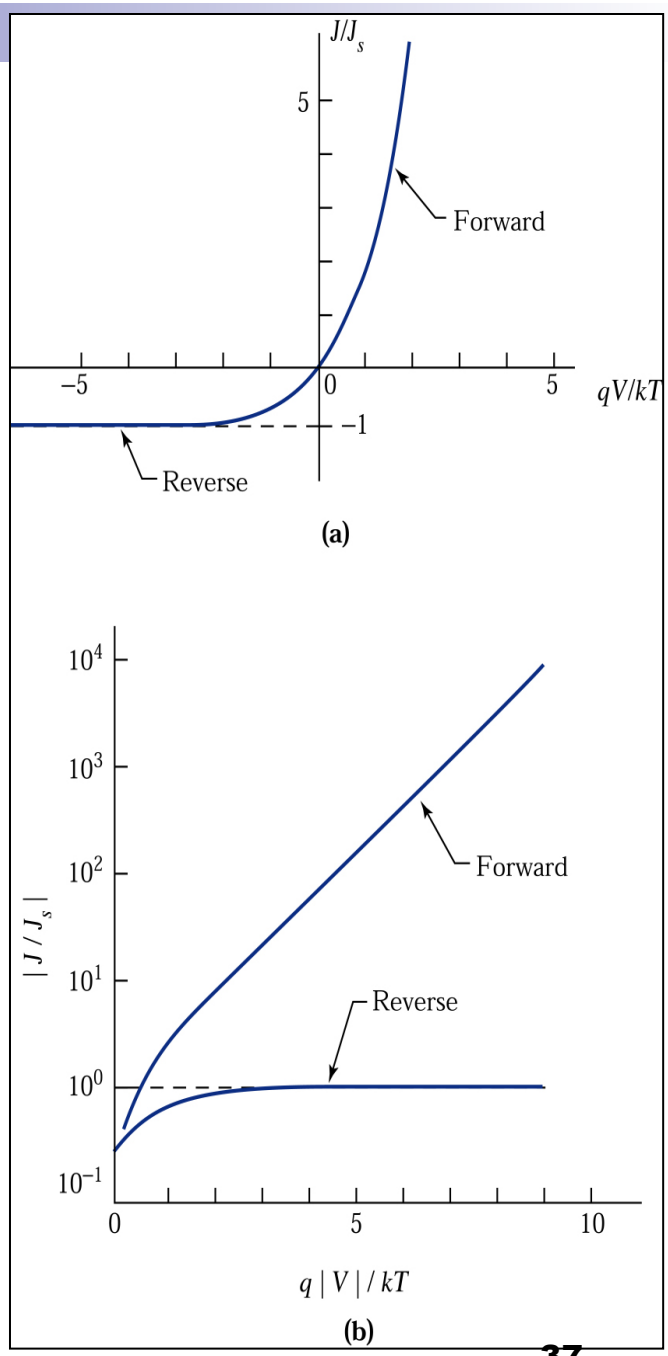
# Rectification

$$J = J_s\left(e^{eV/kT} - 1\right)$$

Under forward bias (V is positive), the current increases exponentially with the voltage.

Under reverse bias (V is negative), the current goes towards the saturation current…

…hence the *p-n* diode is rectifying.



# Junction breakdown

When a sufficiently large reverse bias is applied to a p-n junction, it breaks down and conducts a very large current.

There are 2 mechanisms by which this can occur…

The tunneling effect

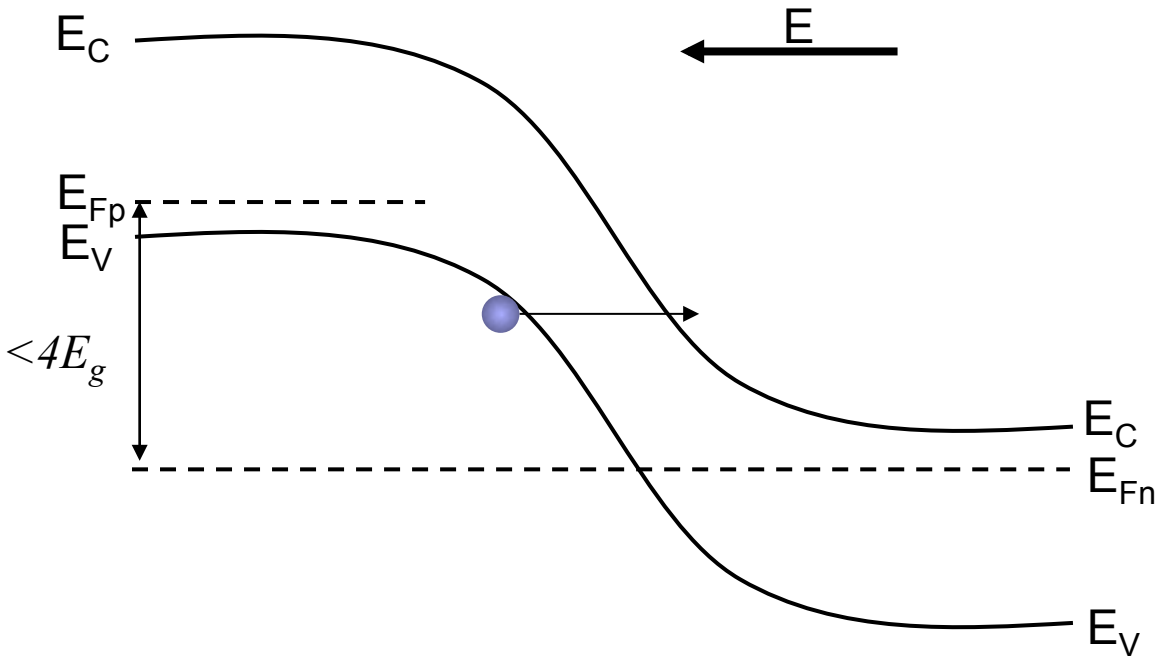
> This is the basis for the tunnel diode and one mechanism for storing and erasing charges in non-volatile semiconductor memory (NVSM) devices

Avalanche multiplication

> This effect imposes an upper limit on the reverse bias in most devices. It limits the collector voltage of a bipolar transistor and the drain voltage of a MOSFET.

# The tunneling effect

When a high electric field is applied to a p-n junction in the reverse direction, an electron can tunnel through the bandgap from the valence band to the conduction band.




Tunneling is the main breakdown mechanism for Si and GaAs junctions where the breakdown voltage is less than $4E_g/e$

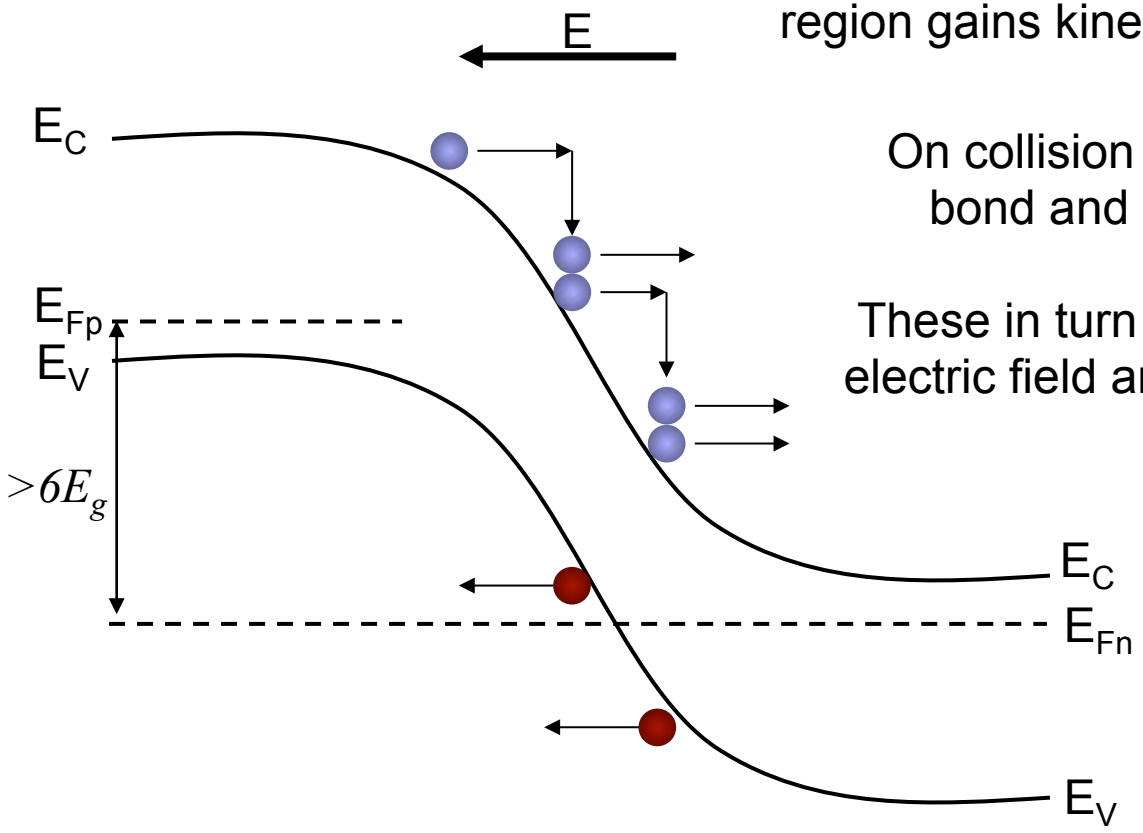
# Avalanche multiplication

Junction breakdown at reverse biases in excess of $6E_g/e$ is dominated by avalanche multiplication…

A thermally generated electrons in the depletion region gains kinetic energy from the electric field

On collision with a lattice atom it breaks the bond and generates an electron-hole pair

These in turn acquire kinetic energy from the electric field and generate more electron-hole pairs…and so it continues.



# Real Diode

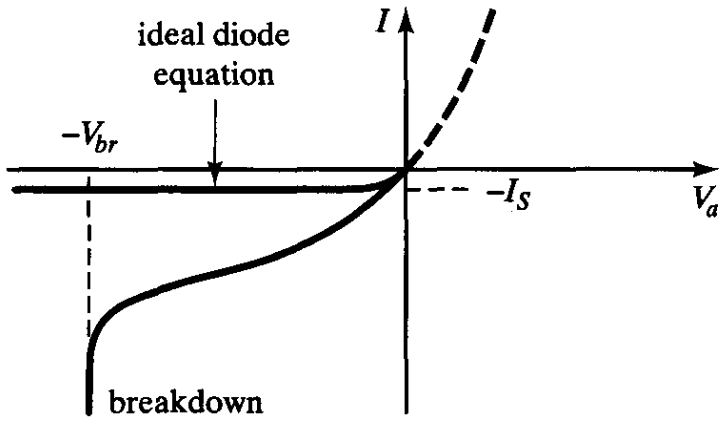
## In ideal diode:

No generation or recombination in the depletion region.

Low level injection under forward bias.

Outside of the depletion region is neutral

# Real Diode




## In real diode:

Under forward bias, excess minority carriers in the depletion region causes recombination to increase.

Under reverse bias, the deficit of minority carrier causes generation current to exceed recombination current.

Under high forward bias, low level injection is no longer valid.

Under high forward bias, the resistance in the semiconductor is not negligible.

# Real Diode (reverse current)

The generation current density is the total generation current in the space charge region:

$$J_{gen} = \int_0^W qGdx = \frac{qn_iW}{2\tau_0}$$

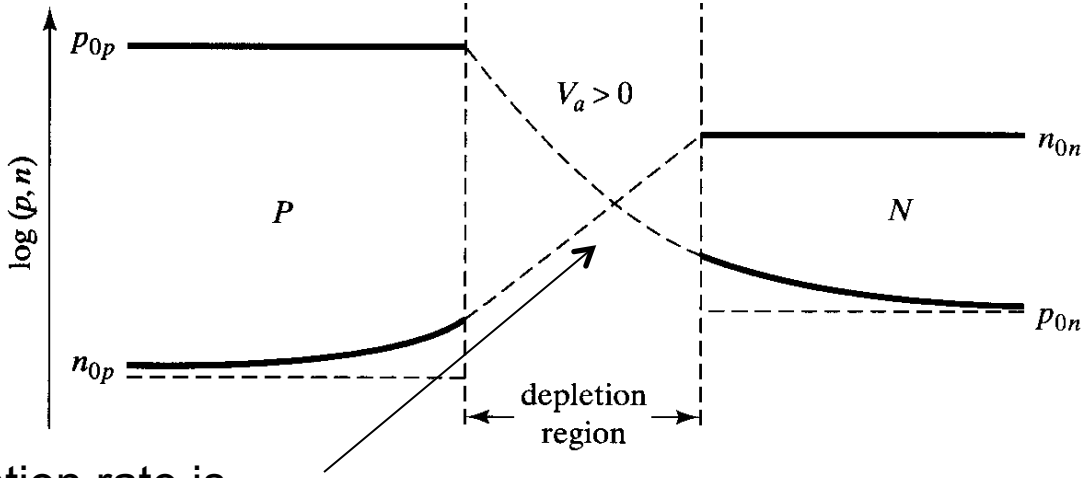
$W$ is a width of space charge region, $n_i$ concentration of charge carriers, $\tau_0$ is an effective lifetime, $G$- generation rate of charge carriers

The total reverse bias current is therefore:

$$J_R = J_S + J_{gen}$$

# Real diode (forward current)

Under forward bias, excess carriers do exist in the space charge region due to the reduced electric field and the large amount of carrier traveling across it. Both the excess electrons and excess hole profiles are decaying across the space charge region but in opposite direction.




Since recombination rate is proportional to the product of excess electron and hole concentration, it must peak right at the point where the two profiles cross each other.

# Real diode (forward current)

If the junction is more or less symmetric, it can be shown that the maximum recombination rate is approximately:

$$R_{\max} = \frac{n_i}{2\tau_0} \exp\left[\frac{eV}{2kT}\right]$$

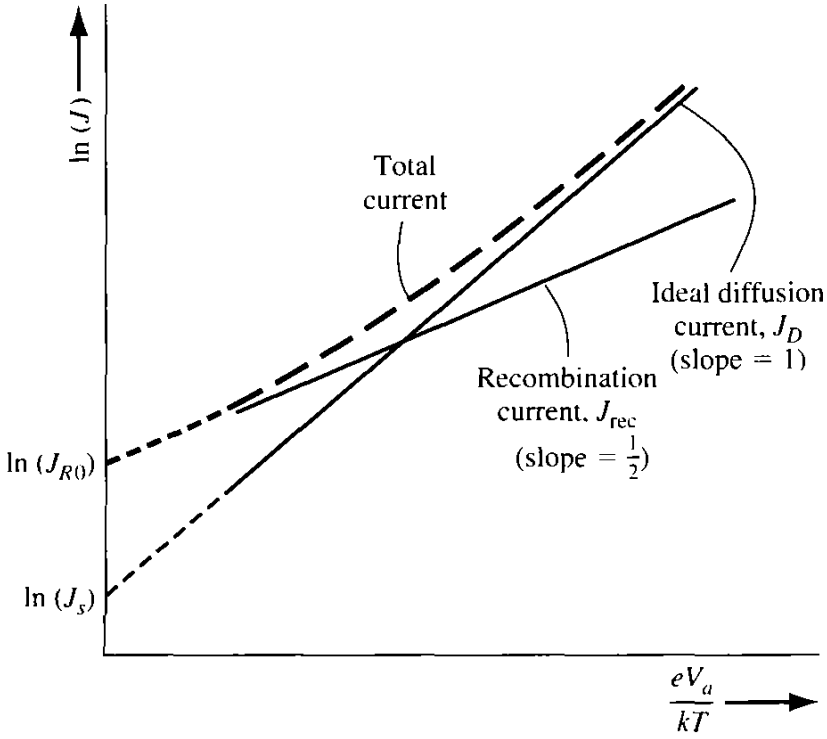
Recombination current is:

$$J_{rec} = \int_0^W eR\,dx = \frac{en_iW}{2\tau_0} \exp\left[\frac{eV}{2kT}\right] = J_{r0} \exp\left[\frac{eV}{2kT}\right]$$

The total forward bias current is:

$$J = J_S\left[\exp\left[\frac{eV}{kT}\right] - 1\right] + J_{r0} \exp\left[\frac{eV}{2kT}\right]$$

# Real diode:




Since

$$J_{gen} = -J_{r0}$$

The total diode current becomes:

$$J = J_S\left[exp\left[\frac{qV_a}{kT}\right] - 1\right] + J_{r0}\left[exp\left[\frac{qV_a}{2kT}\right] - 1\right]$$

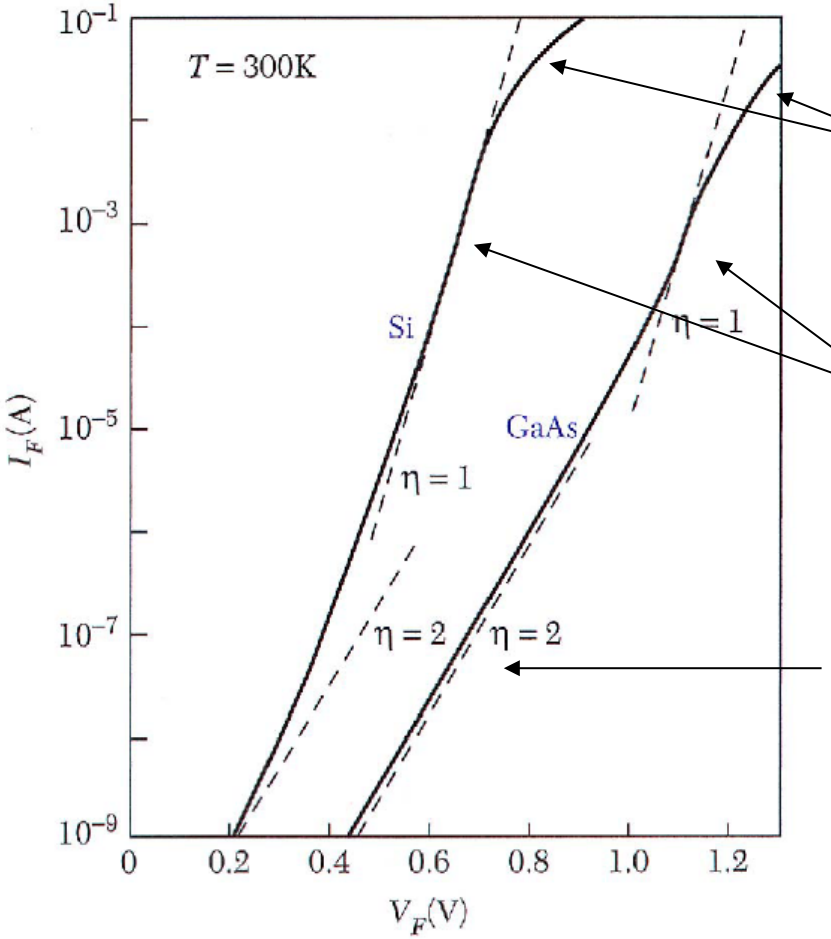
One can rewrite the forward bias current as: $I \propto e^{qV_a/\eta kT}$

where $\eta$ is called the ideality factor.

Its value is 1 when diffusion current dominates and 2 when recombination current dominates.

At low forward bias, when the diffusion current is low and the depletion width is large, forward current is often dominated by recombination current.

# Real diode




**Si and GaAs**

Ohmic region

Diffusion current

Recombination current

# Real diode

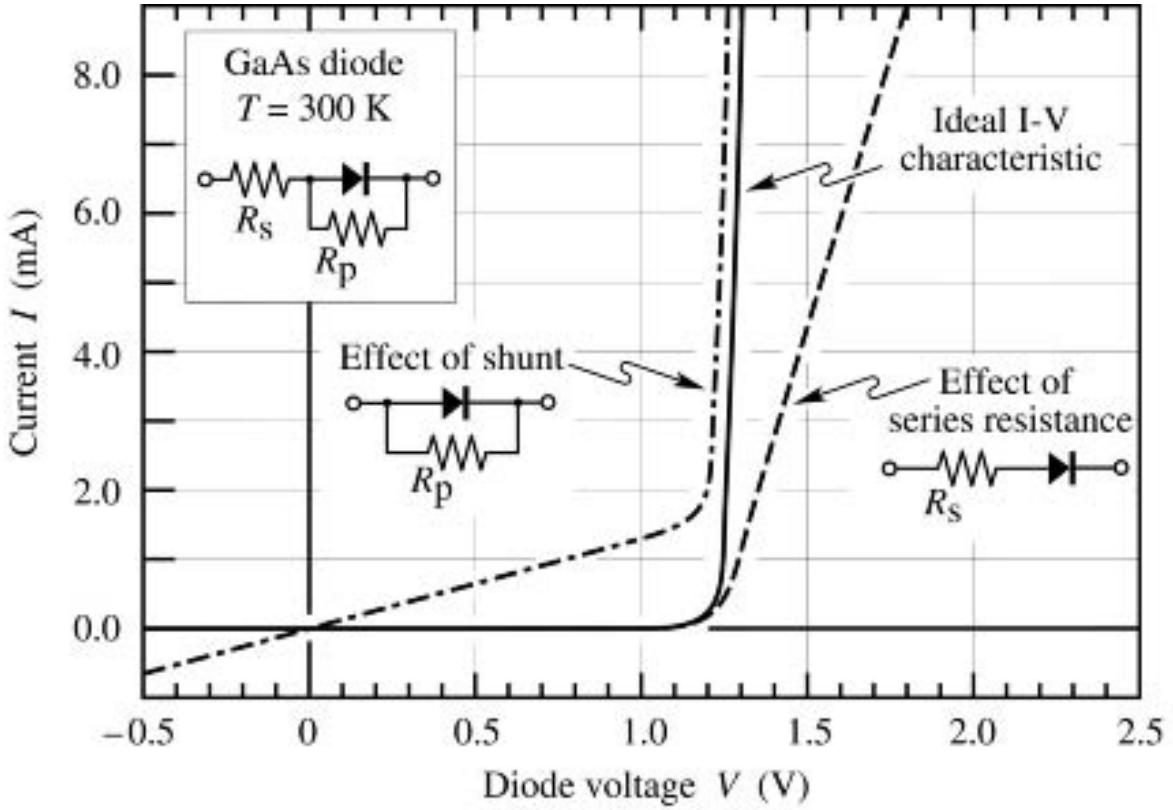
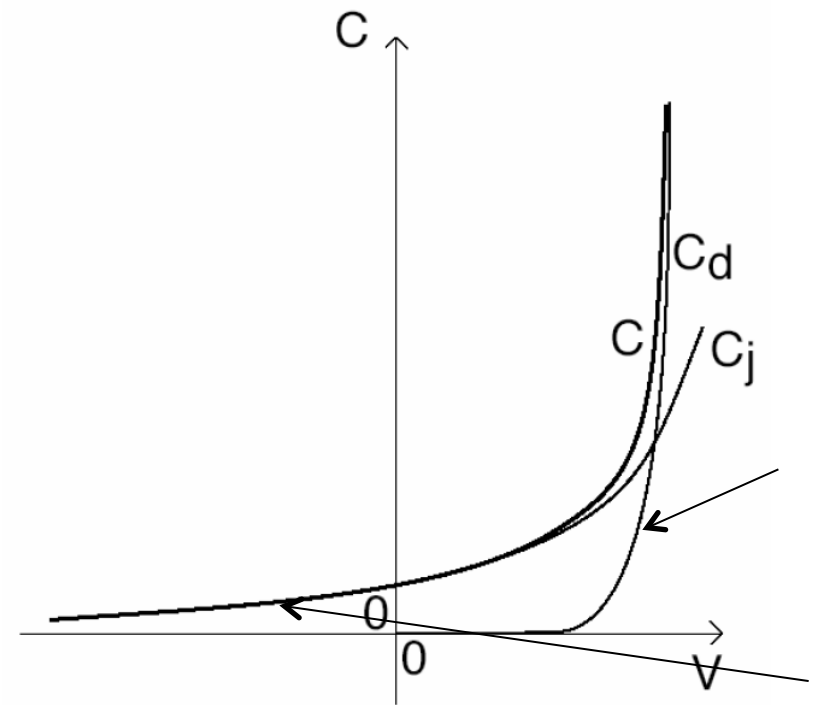



Fig. 3.4. Effect of series resistance and parallel resistance (shunt) on the *I-V* characteristic of a pn-junction diode.

# Capacitance of p-n Junctions

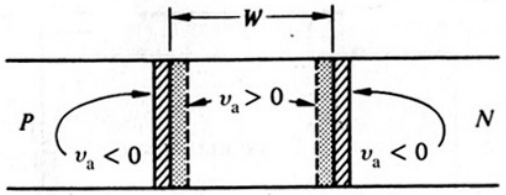



$$C = C_J + C_D$$

- Two types of capacitance in the p-n junction:
  - Junction capacitance $C_j$ arising from the dipole (uncovered - / + charges) in the depletion region
  - Charge storage capacitance $C_d$
- Charge storage capacitance dominates in forward-bias
- Junction capacitance dominates in reverse-bias

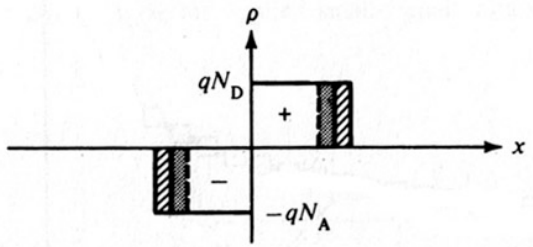
# Junction capacitance (reverse bias)

At reverse bias P-N junction acts like a plate capacitor:




$$C_j = \frac{\varepsilon A}{W}$$

A- area of plates , W- distance between plates




Capacitance: $C = A\frac{dQ}{dV}$

# Junction capacitance

The width of p-n junctions was

$$W = \left[\frac{2\varepsilon}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)\left(V_{bi} - V\right)\right]^{1/2}$$

In case of one-sided junction ($p^+n$ or $pn^+$ or Schottky junction) where $N_B$ is a carrier concentration on low conc. side

$$\longrightarrow \quad = \left[\frac{2\varepsilon}{qN_B}\left(V_{bi} - V\right)\right]^{1/2}$$

Then the capacitance will be:

$$C_J = \frac{\varepsilon A}{W} = A\left(\frac{\varepsilon\, qN_B}{2\left(V_{bi} - V\right)}\right)^{1/2}$$

$C_J \sim N_B^{1/2}$

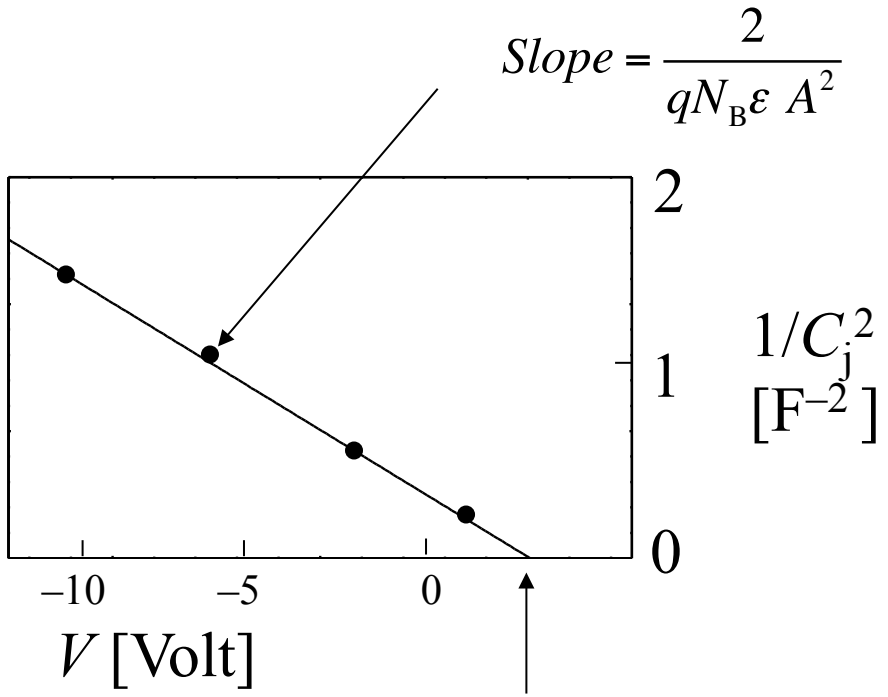
$C_J$ decreases with reverse V

# C-V method

C-V method is used to measure carrier concentration

$$C_J = \frac{\varepsilon A}{W} = A\left(\frac{\varepsilon\, qN_B}{2(V_{bi} - V)}\right)^{1/2}$$

$$\frac{1}{C_J^2} = \frac{2}{A^2 qN_B \varepsilon}(V_{bi} - V)$$

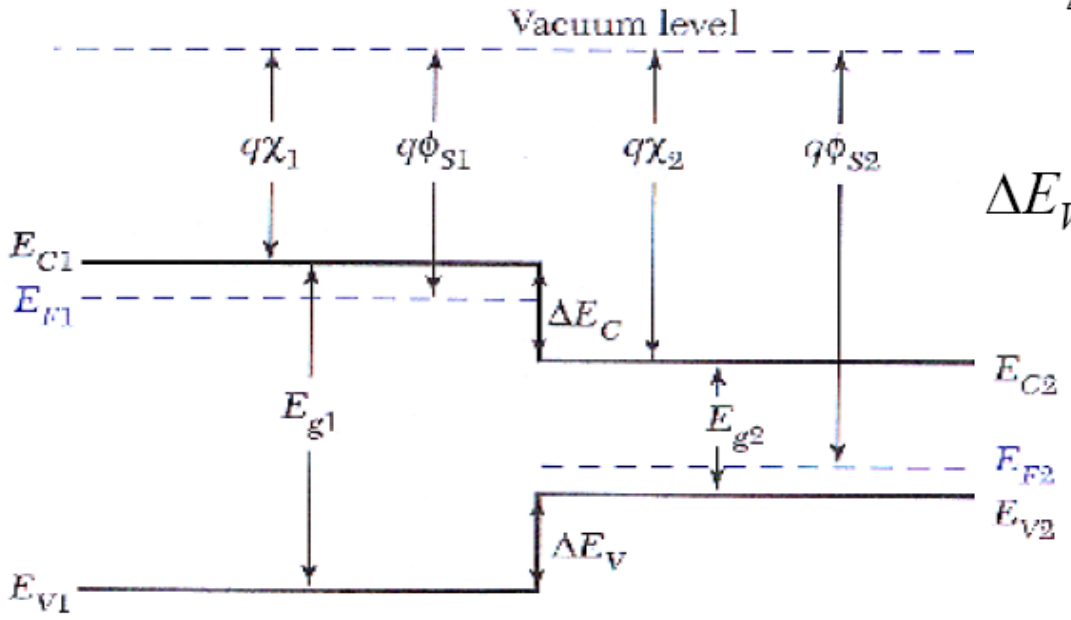



crossing point = $V_{bi}$

# Heterojunctions

2 different semiconductors- heterojunction! (nP, pN, nN, pP)

Before contact formation:



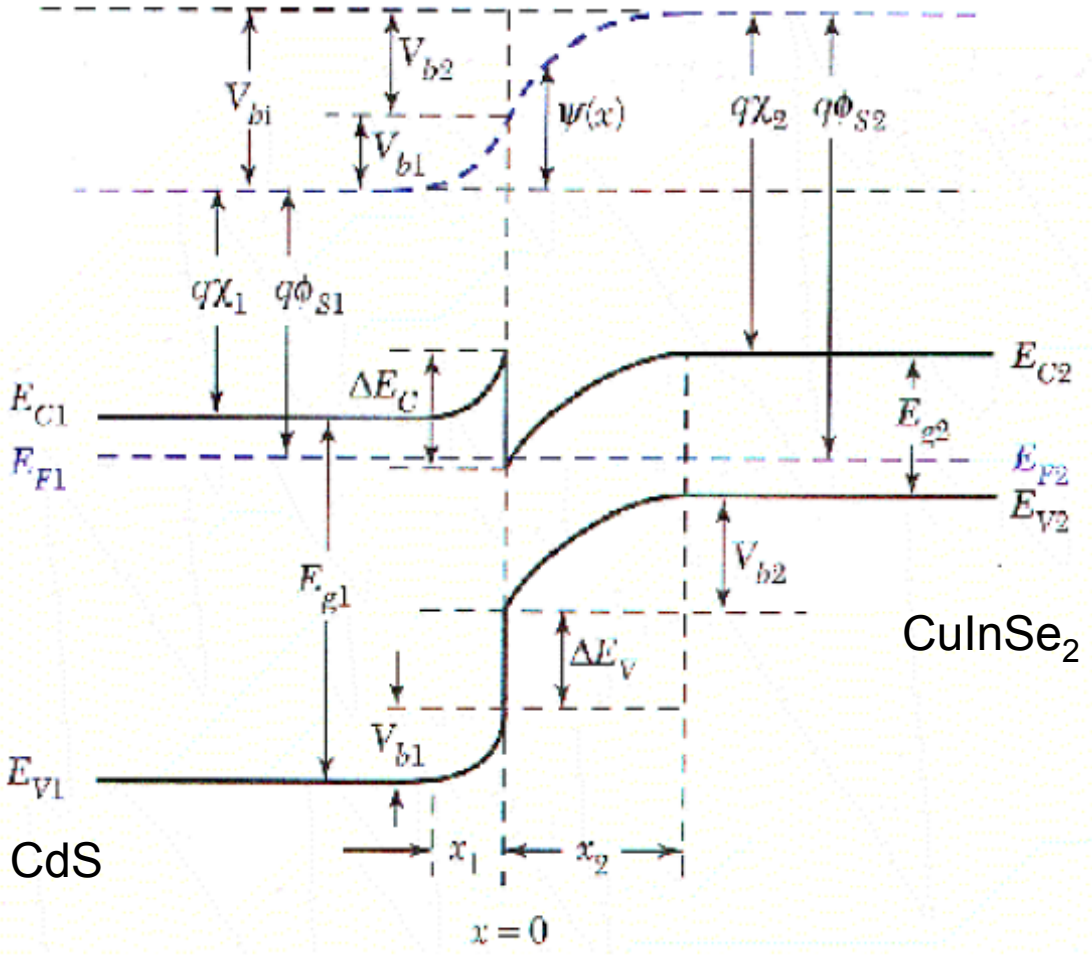

electron affinity

$$\Delta E_C = q(\chi_2 - \chi_1)$$

$$\Delta E_V = E_{g1} + q\chi_1 - (E_{g2} + q\chi_2)$$
$$= \Delta E_g - \Delta E_C$$

# Heterojunctions

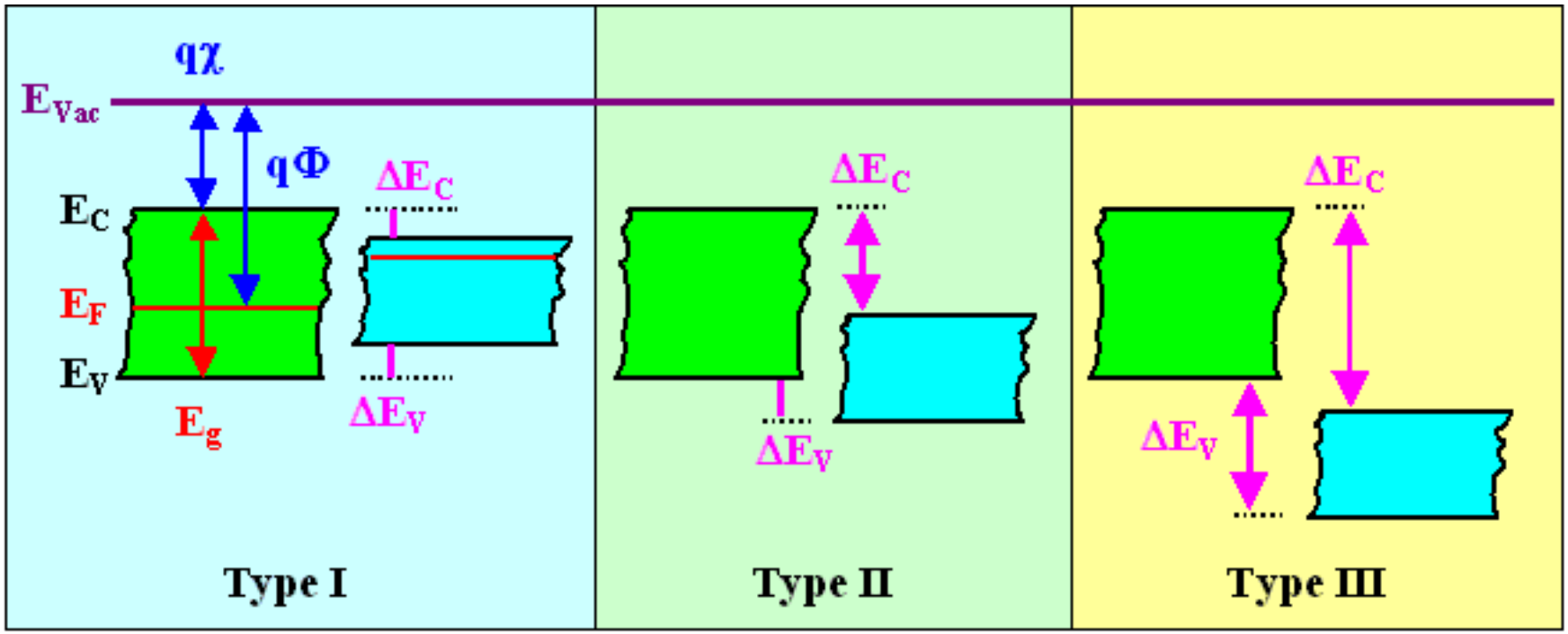
After contact formation:




Built-in voltage:
$V_{bi}=q(\Phi_{S2}-\Phi_{S1})$

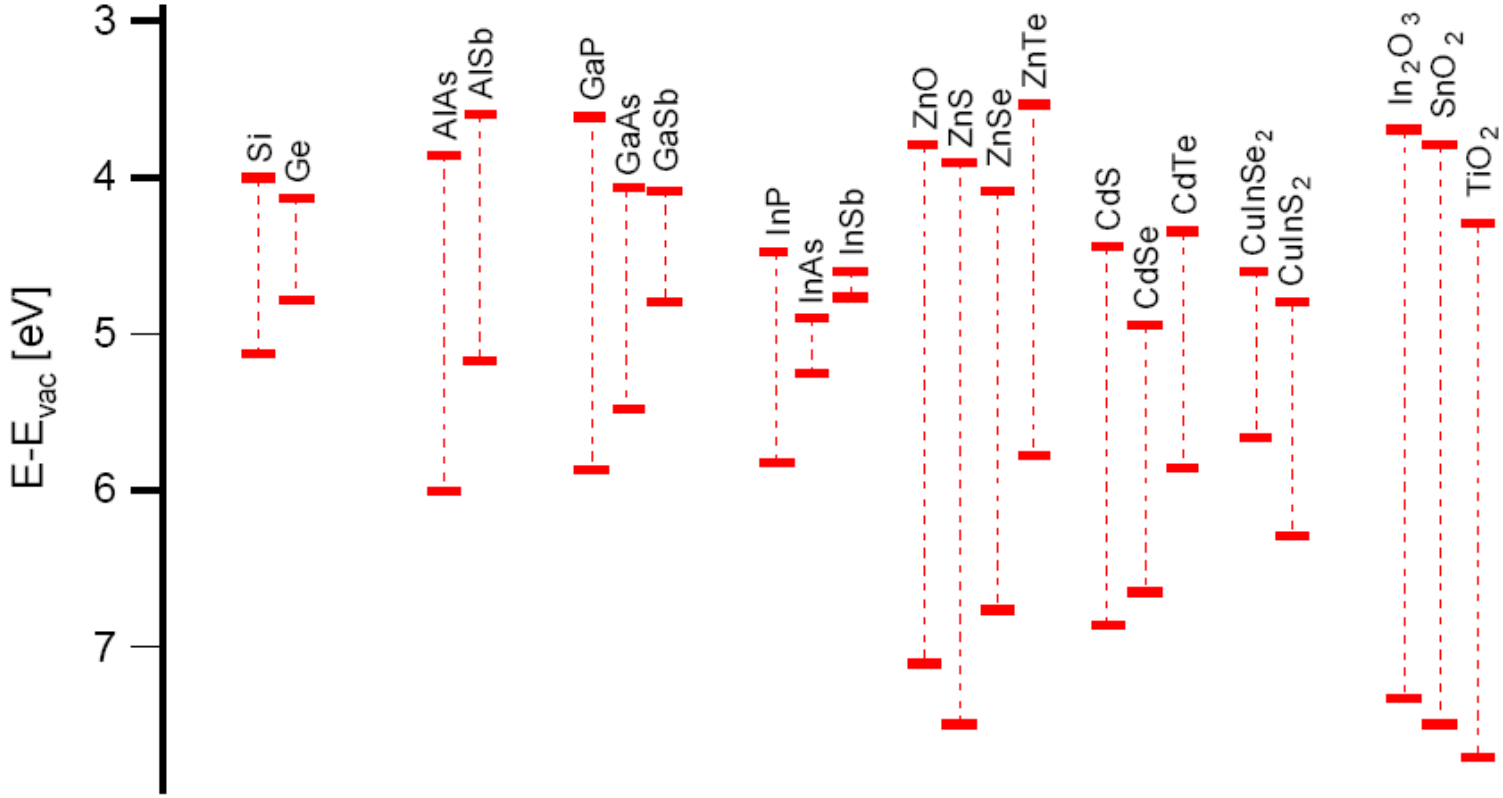
# Heterojunctions

3 main types of heterojunctions:



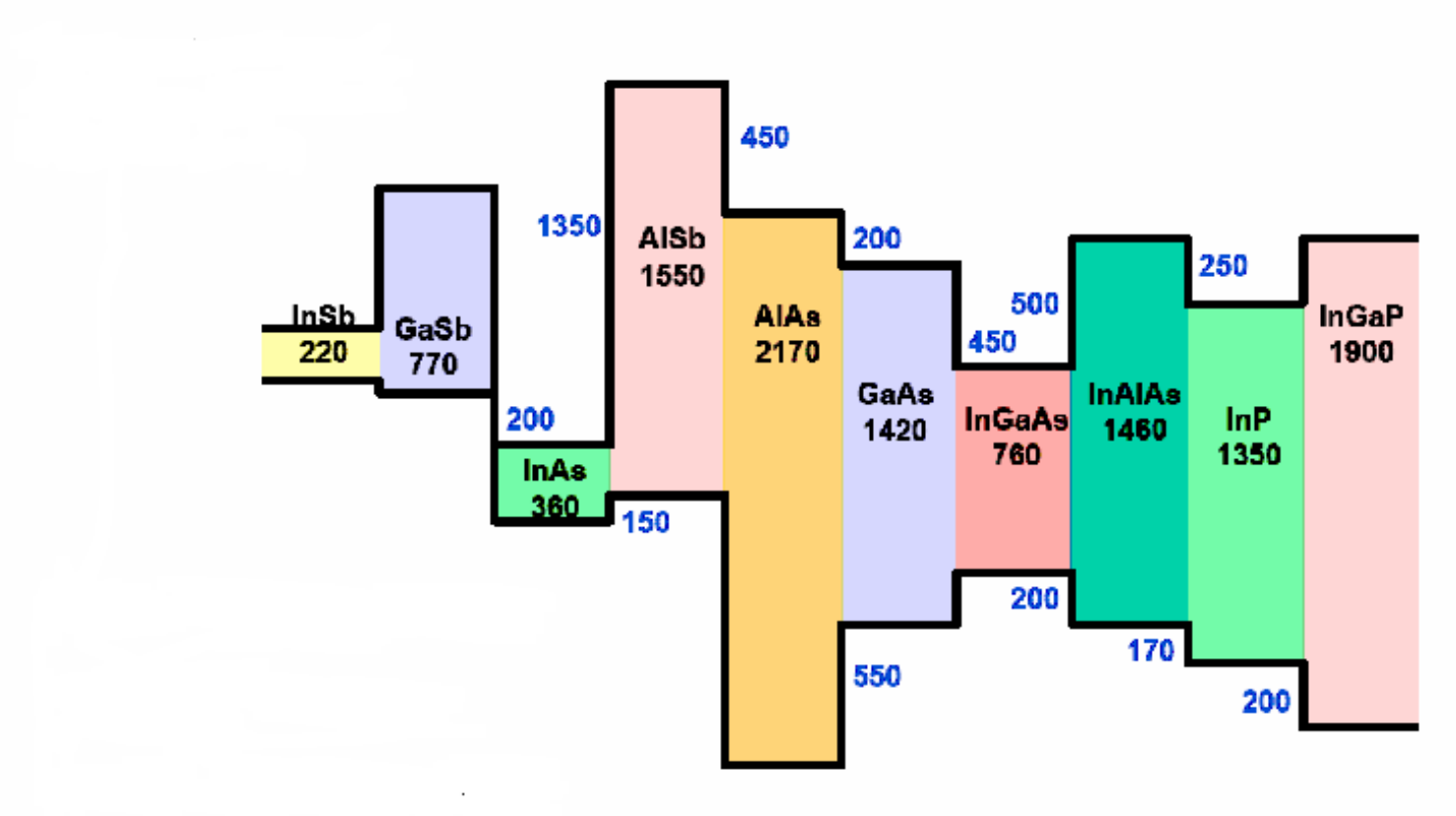
# Heterojunctions

Position of conduction and valence bands for some semiconductors:



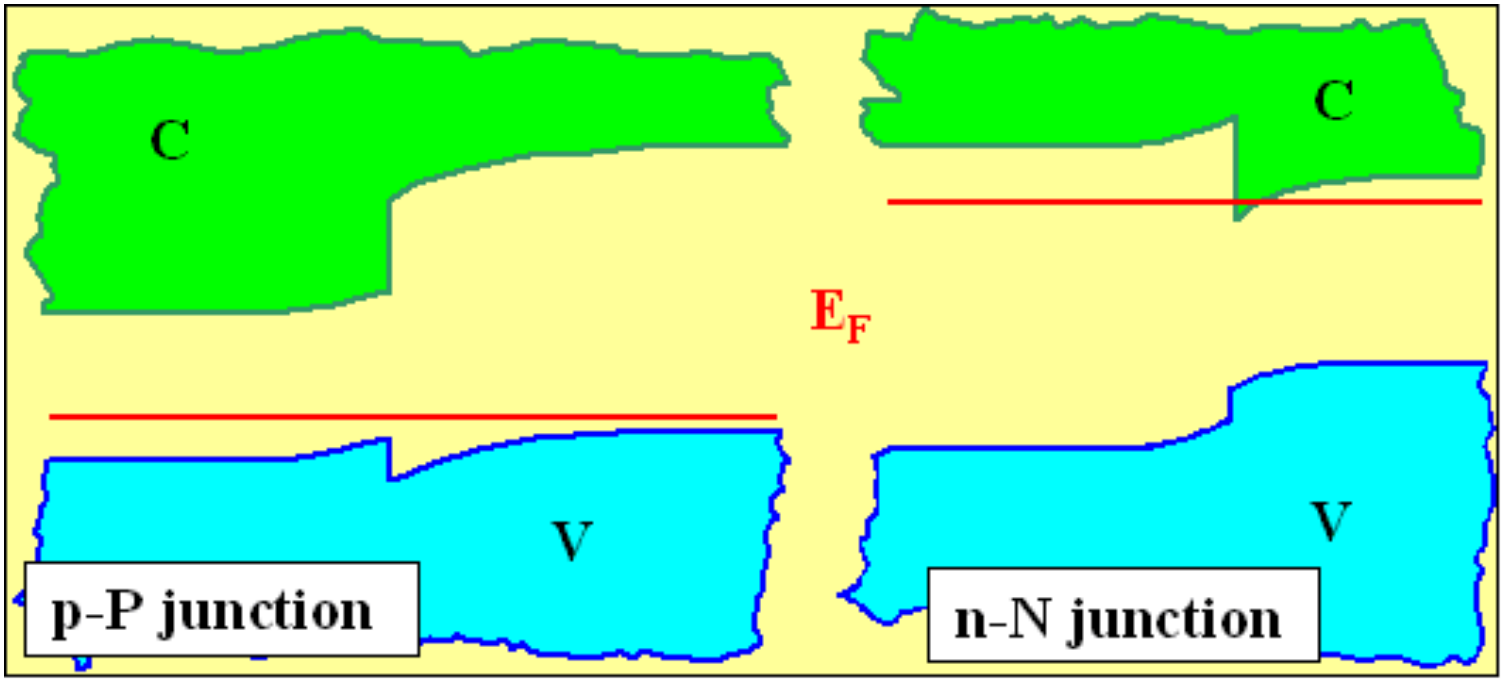
# Heterojunctions

C and V band positions for III-V semiconductors (meV):



# Heterojunctions

n-N and p-P heterojunctions:



# Heterojunctions

Problems:

- ✓2 different semiconductors – different crystal lattice- lot of defects in junction

- ✓the real junction behavior is not clear

- ✓Why heterojunctions? - Light can come in and out easily!